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Polar Charges Induced Electric Hysteresis of ZnO Nano/Microwire for Fast Data Storage

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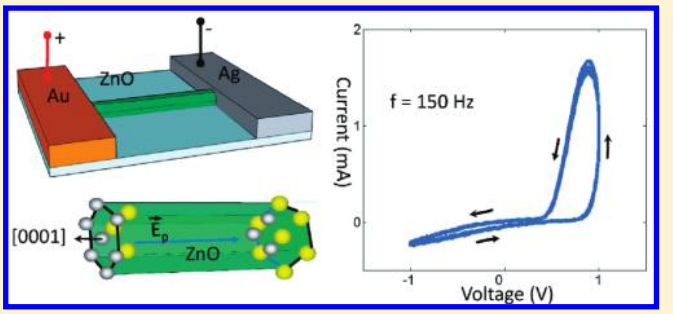
Supporting Information

ABSTRACT: We demonstrate an innovative memory device made of a single crystalline ZnO nanowire/microwire that works with a different mechanism from the p-n junction based memristor. A nonsymmetric, Schottky−Ohmic contacted ZnO nano/microwire can serve as a memristor if the channel length is short and the applied frequency is high. The observed phenomena could be explained based on a screening model of the polar charges at the two ends of the wire owing to the crystal structure of ZnO. The polar charges are usually fully screened by free electrons coming from the metal sides. But when the magnitude of the externally applied field exceeds a threshold value, the free electrons that screen the polar surfaces can be pulled away from the interface region, leading to a transient change in the effective height of the local Schottky barrier height owing to the electrical field formed by the polar surfaces of ZnO nanowires, which acts as a resistor with its magnitude depending on the total charges being transported. Such a phenomenon could be used for high density and fast writing/erasing data storage.



KEYWORDS: Memristor, ZnO nanowire, polar surface, Schottky barrier, memory

Ferroelectric random access memory[1−3] is attracting a great interest both in scientific research and industry applications for its low power consumption, faster reading/writing speed, and extremely large writing-erasing cycles compared to other memory technologies, such as capacitors and transistor-coupled units made by lithography technique on silicon wafers.[4,5] The advantages come from the spontaneous polarization dipoles in the cells of ferroelectric materials, which can be rapidly reversed by an electric field. However, as the size of a memory unit shrinks to submicrometer scale, the ferroelectric material would lose its ferroelectric property due to the surface screening effect, resulting in lower storage density.[6−8] As the traditional random access memory reaches the limit of the metal−oxide−semiconductors, searching for new approach for fast reading-rewriting and high-density memory technology is important for the development of information technology. Here, we report a new memory device fabricated using single crystal ZnO nanowires based on a different working mechanism, which preserves hysteresis in $I-V$ curve from 100 Hz to 10 kHz (theoretically to GHz) ranges and could be an ideal technique for developing ultrafast, high-density data storages.

The device fabrication process is presented in Figure 1a. Intrinsic nonconductive silicon wafer was first coated with a thin layer of SiO_2, then on which a single crystal ZnO nanowire/microwire (NW/MW) was put on by micromanipulator. Nonsymmetric contacts at the two ends of the MW were constructed by depositing gold and silver as electrodes using a double lithography processes to form Schottky[9] and Ohmic[10] contacts, respectively. Figure 1b is a scanning electron microscopy (SEM) image of a typical ZnO MW used in the device fabrication process. The hexagonal shape of the MW indicates its growth direction along ⟨0001⟩. The equipments for current−voltage ($I-V$) characterization of the as-fabricated devices were DS345 signal generator from Stanford Research, MPH probe arm from Cascade Microtech, Infinity Probe, homemade Faraday cage, PCI-6259 DAQ from National Instrument, and computer with Labview 8.2 software. When the $I-V$ characteristics of the device was characterized at low frequency such as 10 Hz with a sinusoidal voltage source, the $I-V$ curve was linear and the current did not depend on the route of the sweeping voltage. Interestingly, as the frequency of the applied voltage increased, the hysteresis loop appeared. Figure 1c shows a typical $I-V$ curve of the device measured at 150 Hz sinusoidal voltage signal with an amplitude of 1 V. The hysteresis $I-V$ curve loop in the negative voltage range clearly shows the device behaving like a typical memristor with current depending on the scanning route of the applied voltage with an on−off value of $\sim 1 \times 10^3$. The whole shape of the curve still shows the asymmetric rectification characteristic of the Schottky-type, which was formed between gold electrode and the n-type ZnO NW, and the hysteresis loop was more pronounced when the Schottky barrier was forward biased. The much reduced hysteresis loop at the reverse bias is possibly due to the corresponding large resistance. One phenomenon must be pointed out is that the hysteresis loop only

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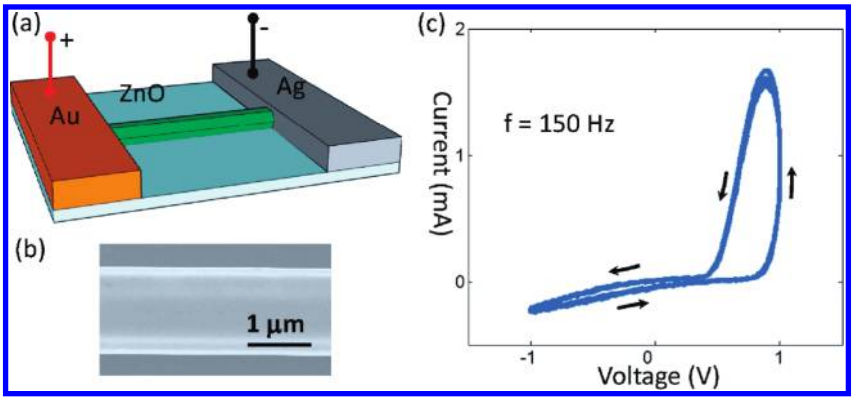

Figure 1. (a) Schematic structure of a memory device fabricated using a single ZnO NW/MW. (b) SEM image of the ZnO MW shows its hexagonal cross-section and the ⟨0001⟩ growth direction. (c) Typical multicycle $I-V$ curves of the ZnO NW/MW device under an applied sinusoidal voltage signal with amplitude of 1 V at frequency of 100 Hz. Hysteresis loops appear in the forward bias.

emerged when the frequency of the applied voltage was larger than a certain value that was normally larger than 60 Hz based on our 16 measured devices with channel length from 5 to 10 μm.

The hysteresis loop becomes even pronounced with the increase of frequency. Figure 2a−c shows the hysteresis $I-V$ curves of a ZnO MW with a length ∼5 μm. As the frequency of the operating voltage increased from 100 Hz to 10 kHz, the hysteresis $I-V$ loop became bigger, especially at the forward biased case. At the reversely biased case, a small loop emerged as the frequency was increased. It is necessary to point out that the hysteresis loop presented here is different from that generated due the capacitance of the whole measurement system, which is normally an elliptical shape loop rather than a crossed/twisted loop, so that the $I-V$ curve may not go through the origin. From Figure 2 panels b to c, the hysteresis loop in the negative biased voltage range is stronger than that produced by the measurement system.

The size of the hysteresis loops depends on the length of the MWs used for the devices. For the MWs with channel lengths longer than 100 μm, the measured $I-V$ curve showed little hysteresis behavior (Figure 2d). This is a rather surprising phenomenon.

To see if a single crystal structure of the microwire is indispensible for observing the hysteresis loop, we have fabricated devices using polycrystalline ZnO stripes made using lithography and sputtering process on a Si substrate with the same geometry (10 μm in length) and identical fabrication process as the devices shown in Figure 1. The polycrystal ZnO MW has the similar parameters with single crystal NW/MW, but has no polar surfaces. $I-V$ measurements at 1 V and at 100 Hz indicated no observable hysteresis loop (Figure 2e). The same measurement was performed on a normal 1 mega Ohm axial-lead resistor and the linear $I-V$ curve without any hysteresis loop is shown in Figure 2f.

Our experiments show that the following conditions need to be met to observe the hysteresis loop shown in Figure 1b: a single crystal ZnO wire growing along ⟨0001⟩; a higher frequency; and shorter channel lengths. But such phenomena cannot be explained using the memristor effect, as presented in follows.

Recently, hysteresis loops with shapes similar to those shown in Figure 1 have been explained as the memristor effect.[11,12] Memristor is a two-terminal device whose resistance depends on the total charges having been transported through it.[13] Most of the memristors that have been demonstrated are made of sandwiched structures of electrodes and two layers of semiconductors with different doping levels.[14−16] The different concentrations of carriers, such as ions or electrons, move with different mobilities under the applied electric field, which causes the drift of p-n boundary between the different doping materials and thus forms the hysteresis shape $I-V$ curve. Although the memristors are still in their proving of concept stage, the potential applications and broad impacts in memory technique are anticipated. The carriers in such a memristor have a rather low mobility. Therefore, the magnitude of the memristor effect should not sensitively depend on the channel length along which the charges will be transported, and more importantly, the size of the hysteresis loop is expected to be largely reduced with the increase of the frequency at which the external voltage is applied. These characteristics for memristor are in contrast to the data received for our devices. Therefore, the origin for the observed hysteresis loop in Figures 1 and 2 is likely different from that proposed mechanism for the memristor.

The mechanism for memory devices might be related to the polar surfaces of ZnO NW/MW. There are two components of contributors to the conducting channels at the interface: the end surface of the wire and its side surface. If the area of contact for the side surface with the electrode is not too large in comparison to that of the end surface, considering the distribution of the carriers across the wire (see Supporting Information), the current that is transported through the end surface of the wire is substantially significant for the entire structure. Thus, this component may be responsible to the effect/change we have observed here, while the current transported through the side surface may show little memristor effect, which will contribute to the baseline current and will not be discussed here.

Our model is thus constructed based on such an assumption and considering only the end polar surfaces. The single crystal ZnO NW, synthesized by high-temperature vapor deposition method, has grown direction along c-axes. Owing to the unique wurtzite structure of ZnO, strong polar surfaces form at the two ends terminated with Zn^{2+} cations and O^{2-} anions, respectively. The presence of the polar surfaces in ZnO nanobelts[17] at the side surfaces is the cause of forming various unique nanostructures, such as nanohelix,[18] nanoring,[19] and nanospring,[20] owing to the ionic charges on the polar surfaces. As for the hexagonal shape nanowires, the polar surfaces are at the ends, which are schematically shown in Figure 3a. The polar surfaces form an internal electrical field along c-direction. At ambient environment, the polar surfaces

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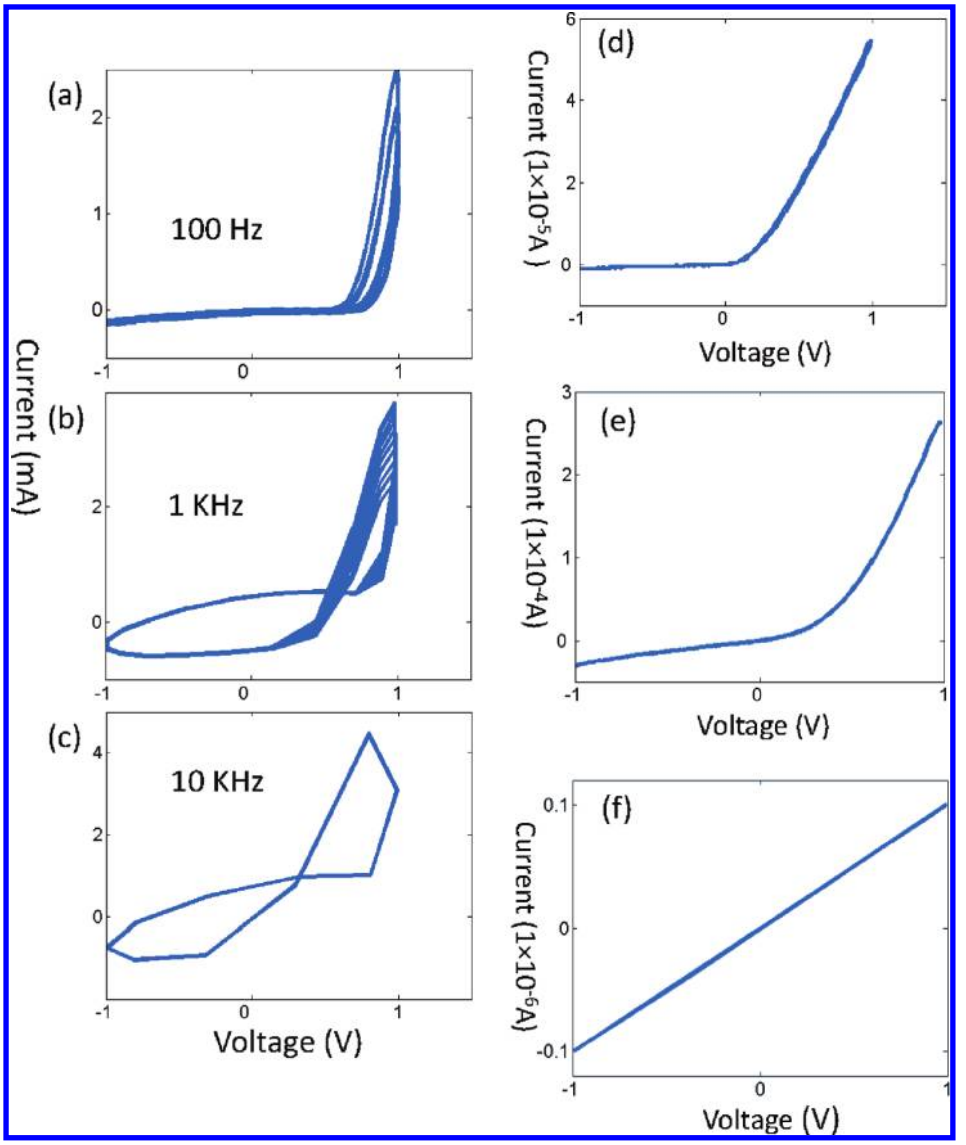

Figure 2. $I-V$ curves of a ZnO NW/MW memristor with the increase in frequency of the applied voltage signal. The amplitude of the voltage signal keeps at 1 V: (a) 100 Hz; (b) 1 kHz; (c) 10 kHz. $I-V$ curves of the same type of device structure but made using different materials; the applied voltage signal is a 100 Hz sinusoidal at amplitude of 1 V. (d) $I-V$ curve of 100 μm long ZnO single crystal wire. (e) $I-V$ curve of 10 μm long polycrystalline ZnO wire. (f) $I-V$ curve of a 1 MOhm axial-lead resistor.

are likely to be screened or neutralized by surface adsorbents. During the device fabrication and the deposition of electrode at relatively high temperature, the adsorbed molecules tend to be desorbed, resulting in a good contact between Au and ZnO. The free electrons in Au tend to migrate toward the interface region to screen the polar charges within a very short period of time. If the magnitude of the applied voltage is small, the distribution of the electrons at the interface will not be affected, thus, no hysteresis loop would be observed. If the magnitude of the applied voltage is larger than a threshold voltage, the local field is large enough to pull the electrons away from the interface, but the polar charges remain. In such a case, the transient current depends on not only the magnitude of the instantaneously applied potential but also the "history" of the applied voltage. If the channel length is increased, the local electric field would be reduced at a fixed applied voltage and the size of the hysteresis loop would be reduced. If there are no polar charges at the interface, no electrons are required to screen them, thus, there would be no hysteresis effect.

If the frequency of the applied voltage is low, the n-type doping in the MW could be mobile quickly enough to supplement the effect of the screening electrons, so that there is no observable or much reduced hysteresis loop in the $I-V$ curve although the magnitude of the applied voltage is high. If we increase the frequency of the applied voltage, the mobility at which the n-type doping can transport may not be high enough to instantaneously compensate the high mobility of the free electrons at the interface. The dependence of the local resistance on the voltage becomes stronger, resulting in a large size hysteresis loop, as observed in Figure 2a−c.

In consideration of the work function of the metal electrode and the electron affinity of ZnO, a Schottky and Ohmic contact would be formed between gold and silver with ZnO, respectively.

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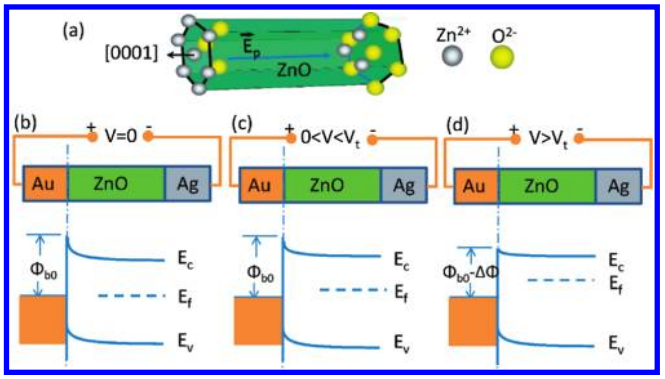

Figure 3. (a) Schematic diagram of a ZnO wire along *c*-axes direction with polar surfaces on ±(0001) surfaces terminated with Zn^{2+} and O^{2-} ions, respectively. (b) Band structure at the interface of the ZnO NW/MW and gold electrode when there is no external electric field being applied. (c) Band structure change at the interface of ZnO NW/MW and gold electrode when the external electric field is less than the threshold electric field E_0 required for pulling the screening electrons. (d) Band structure change at the interface of ZnO NW/MW and gold electrode when the external electric field is larger than E_0. The Schottky barrier is further lowered with the increase of internal electric field formed by the polar surfaces.

Most of the resistance of the device is from the Schottky barrier at Au−ZnO interface. The Schottky barrier energy band diagram is shown in Figure 3b. When an external electrical field is applied but its magnitude is less than the threshold value E_0, the band structure is shown in Figure 3c. The Fermi level of the electrons in gold is increased and the Fermi level in ZnO will match that of gold, which leads to the bending of the conduction band and valence band of ZnO. When the applied electrical field increases to a threshold value ($|E| > E_0$), the screening charges are pulled and begin to move away from the polar surface, and the corresponding band structure is shown in Figure 3d. The net total charge density (polar charges and screen charges) at the polar surface is given by

$$\frac{d\sigma(t)}{dt} = \mu E(\sigma_0 - \sigma(t)) \tag{1}$$

where μ is the mobility of the screening charges (electrons at the positive polarization charges side and positive ions or holes at the negative polarization charge side), E is the electric field, σ_0 is the local screening charge density without applied electrical field. For simplicity, suppose that the electric field and the mobility are constants; then the solution of eq 1 is

$$\sigma(t) = \sigma_0(1 - e^{-\mu E t}) \tag{2}$$

While the surface charges fade away, the net charges at the polar surfaces of ZnO nanowire will increase from zero to σ_0. The change in Schottky Barrier Height (SBH) is given by[21]

$$\Delta\phi_b = \frac{\sigma_{pol}}{D}\left(1 + \frac{1}{2q_S w_d}\right)^{-1} \tag{3}$$

where σ_{pol} is the volume density of the polarization charges (in units of the electron charge q), which is given by $\sigma_{pol} = \sigma/q$, D is a two-dimensional density of interface states at the Fermi level in the semiconductor band gap at the Schottky barrier, and w_d is the width of the depletion layer. Associated with the states in the band gap at the interface is a two-dimensional screening parameter $q_S = (2\pi q^2/k_0)D$, where q is the electronic charge and k_0 is the dielectric constant of the semiconductor. Furthermore, the current in Schottky contact is[22]

$$I_j = SA^{**}T^2 \exp\left(-\frac{\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{4}$$

where S is the area of the Schottky contact, A^{**} is the effective Richardson constant for thermionic emission, T is the temperature, q is the electron charge, k is the Boltzmann constant, V is the applied voltage, and ϕ_b is the SBH of the Schottky contact. While applied voltage is zero, the SBH of the Schottky contact is ϕ_{b0} in thermal equilibrium. Considering $\phi_b = \phi_{b0} + \Delta\phi_b$ and substituting eq 3 into eq 4

$$I_j = SA^{**}T^2 \exp\left(-\frac{\phi_{b0}}{kT}\right)\exp\left(-\frac{2q_S w_d \sigma_{pol}}{(1 + 2q_S w_d)D}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{5}$$

The term $\exp\{-(2q_S w_d \sigma_{pol})/[(1 + 2q_S w_d)D]\}$ depends on the electric field and time due to term σ_{pol}. When the applied voltage is a periodic signal, such as $v_0 \sin(\omega t)$, $I-V$ curve displays obvious hysteresis in the case of forward bias. In the case of reverse bias, the effect is smaller than the forward bias due to the high resistance and much smaller current. The above model schematically describes the $I-V$ curve shape of the memristor device as shown in Figure 1c.

On the basis of the model above, we carried out the simulation of the $I-V$ curve for the device with ZnO NW length of 5 μm and radius of 0.5 μm. The relative dielectric constant is $k_0 = 8.91$. The effective Richardson constant is $A^{**} = 32\ A\cdot cm^{-2}\cdot K^{-2}$. We take $w_d = 20$ nm, $D = 1.0 \times 10^{-14}\ (eV\cdot cm^2)^{-1}$, electrons mobility is 200 $cm^2/(V\cdot s)$, and $T = 300\ K$, which are the typical values obtained from the experiments. The applied electric field $E = 1.0 \times 10^6$ V/m, $\sigma_0 = 3.0 \times 10^{-5}$ C/m^2 and $\phi_{b0} = 0.6$ eV. The amplitude of the applied voltage is 1 V at a frequency of 2000 Hz. The calculated $I-V$ curve shows an asymmetric shape like a typical Schottky contact (Figure 4a). In the part of reversely bias, the curve shows no hysteresis loop. Significant hysteresis loop appears in the forward biased part, which is in agreement to the experimental data (Figure 1c). If the ZnO NW is relatively long, which means that the resistance increases significantly, the effect of the fading screening charges on the polar surface is weak in contributing to the overall resistance and thus the hysteresis characteristic fades out. Figure 4b is the simulation of the theoretical $I-V$ curve of such device with a resistance 2 orders larger than the device shown in Figure 4a. The hysteresis loop vanishes and the curve shows a typical Schottky type asymmetry shape.

Current ferroelectric memory technology is limited by the storage density by the minimum domain sizes and width of domain boundaries, because the surface screening effect screens the ferroelectric property. In contrast, the memory device based on piezoelectric single crystal NW/MW takes advantage of the screening charges on the polar surfaces and the amplifying function of the Schottky barrier, which enable a single crystal ZnO NW/MW memory device with ultrahigh storage density because it is feasible to largely reduce the size of the nanowires both in diameter and length. The polar charges at the surface preserves even when the size of the nanowires is at nanometer scale because the polar surface is entirely determined by the crystal structure of ZnO. Furthermore, ZnO single crystal

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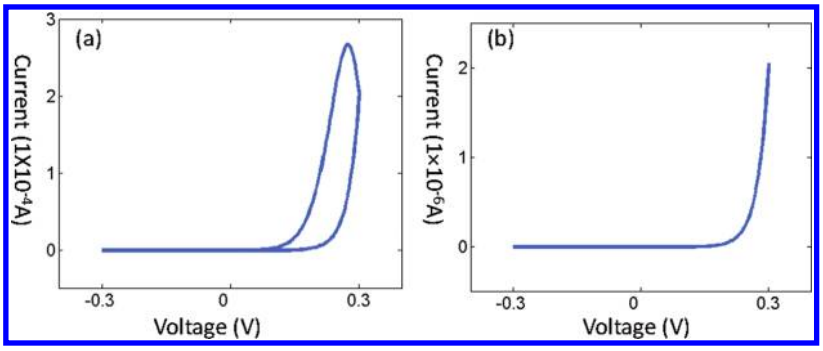

Figure 4. Simulation results using the proposed model. (a) Calculated $I-V$ curve shape of a short ZnO NW/MW memristor based on the polar surfaces model. A prominent hysteresis loop shows in the positive voltage part. (b) Calculated $I-V$ curve shape of a long ZnO NW/MW memristor based on the polar surfaces mode. The hysteresis loop is small due to the large resistance of the long wire.

NW/MW memristor could work at high frequency. The electrons can quickly move to and from the polar surface regions at fast speed and within short distance, which is good for fast data storage/erasing. The major carriers are electrons and gold electrode provides infinite electrons, which lead to almost no carrier depletion zone at the interface. Different from p-n junction-based memristor, the Schottky barrier can work at ultrahigh frequency range (theoretically to GHz range[23,24]). Combining those two novel characteristics, memory units based on single crystal ZnO NW/MW are potential for fabricating high density and ultrafast memories.

In summary, our experiments show that a nonsymmetric, Schottky-Ohmic contacted ZnO nano/microwire can serve as a memristor if the following requirements are met: a single crystalline ZnO wire growing along ⟨0001⟩; a higher frequency of the applying voltage; and shorter channel lengths (wire length). The observed phenomena could be explained based on a screening model of the polar charges at the two ends of the wire that are produced by the crystal structure of ZnO. The polar charges are usually fully screened by free electrons coming from the metal sides. But when the magnitude of the externally applied field exceeds a threshold value, the free electrons that screen the polar surfaces can be pulled away from the interface region, leading to a change in the effective height of the local Schottky barrier owing to the electrical field formed by the polar surfaces of the ZnO NW/MW, which acts as a resistor with its magnitude depending on the total transported charges. The observed memristor hysteresis loop in the $I-V$ curve follows a mechanism that is different from the p-n junction memristor or ferroelectric RAM, and it could serve as high density and fast writing/erasing memory units. The almost nonexisting depletion zone of the electrons and their large mobility in single crystal ZnO NW/MW make this memory device applicable as high-speed memory devices possibly up to gigahertz. Since the polar charges are still present and their very localization is at the interface region, the size of the memory unit can be very small in the range of tens of nanometers by using ultrasmall single crystalline nanowires.

■ ASSOCIATED CONTENT

Supporting Information. Additional information and figure. This material is available free of charge via the Internet at http://pubs.acs.org.

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