Supporting Information

Strain-gated piezotronic logic nanodevices

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Experimental section

Fabrication of the strain-gated inverter (SGI) The SGI was fabricated by bonding two ZnO NWs laterally on a Dura-Lar film. The thickness of the Dura-Lar film is 0.5 mm. The ZnO NWs were synthesized via a physical vapor deposition method reported elsewhere [32] and typically have diameters of 300 nm and lengths of 400 μm (Fig. 1a). The films were first cleaned with acetone, isopropyl alcohol and DI water by sonication, after which, the Dura-Lar films were dried by nitrogen gas blowing. One ZnO NW was placed flat on the top surface of the Dura-Lar film first using a probe station (Cascade Microtech, Inc.) under an optical microscope (Leica Microsystems, Inc.). Silver paint (Ted Pella, Inc.) was applied at both ends of the ZnO NW for electrical contacts. The second ZnO NW was placed on the bottom surface of the Dura-Lar film in the same way.

Experimental setup for strain-gated logic devices A function generator (Model No.: DS345, Stanford Research Systems, Inc.), a low-noise voltage preamplifier (Model No.: SR560, Stanford Research Systems, Inc.) and a low-noise current preamplifier (Model No.: SR570, Stanford Research Systems, Inc.) were used for electrical measurements. One end of the Dura-Lar film substrate was fixed. A linear guided actuator (LinMot, Inc.) was employed to provide mechanical strains in the strain-gated devices.

Noise margin of the ZnO-NW SGI

ε_{IL} and ε_{IH} are defined as pseudo unity gain points on SVTC curve for the following considerations. Assume there is noise perturbations on gate input strain ε_g

$$V_{out} = f(\varepsilon_g + \varepsilon_{noise})$$

Using first-order approximation and Taylor series expansion:

$$V_{out} = f(\varepsilon_g) + (\mathrm{d}V_{out}/\mathrm{d}\varepsilon_g)\,\varepsilon_{noise}$$

If the absolute value of pseudo gain $(\mathrm{d}V_{out}/\mathrm{d}\varepsilon_g)$ is larger than 1, noise signal will be "amplified" and might compromise the SGI performance.

If the absolute value of pseudo gain $(\mathrm{d}V_{out}/\mathrm{d}\varepsilon_g)$ is smaller than 1, noise signal will be "filtered" and hence the obtained logic low input and logic high input regions ensure the gain of SGI operating within these two regions is smaller than 1.

Calculation of strain for ZnO strain gated logic devices

Since the mechanical behavior of the Dura-Lar film substrate is not affected by the ZnO wire due to the much smaller sizes of ZnO NWs, a simple estimation of the strain induced in the ZnO NWs can be obtained using the Saint-Venant theory for small deflections (s2). The shape of the plastic substrate can be approximated as a beam, with thickness $2a$, width w and length l.

For easiness of derivation, the origin of the coordinate system is set at the center of the cross section of one side of the film, while the z axis is parallel to the length l and x axis is parallel to the width w. In order to determine how the NW deforms as the substrate is deflected under an external bending force f_y, only the ε_{zz} component of the strain tensor needs to be calculated, where $\varepsilon_{zz} = \Delta L_{\mathrm{wire}}/L_{\mathrm{wire}}$. Meanwhile, $\sigma_{zz} = -f_y/I_{xx}y(l-z)$, $\sigma_{xx} = \sigma_{yy} = 0$, where I_{xx} is the geometrical moment of inertia for the beam cross section. Therefore, $\Delta L_{\mathrm{wire}}/L_{\mathrm{wire}} = \varepsilon_{zz} = \sigma_{zz}/E$. The lateral deflection D_{max} of the substrate is experimentally easier to measure than the bending force f_y and the relationship between D_{max} and f_y is $D_{max} = f_y l^3/3EI_{xx}$. Therefore (s3)

$$\varepsilon_{zz} = -3\frac{y}{l}\frac{D_{\max}}{l}\left(1-\frac{z}{l}\right)$$

With $y = \pm a$ and $z = z_0$ is the vertical distance between the fixed end of the Dura-Lar film substrate and the middle point of the ZnO NW. The positive and negative sign for y stand for the compressed side and tensile side of the beam, respectively.

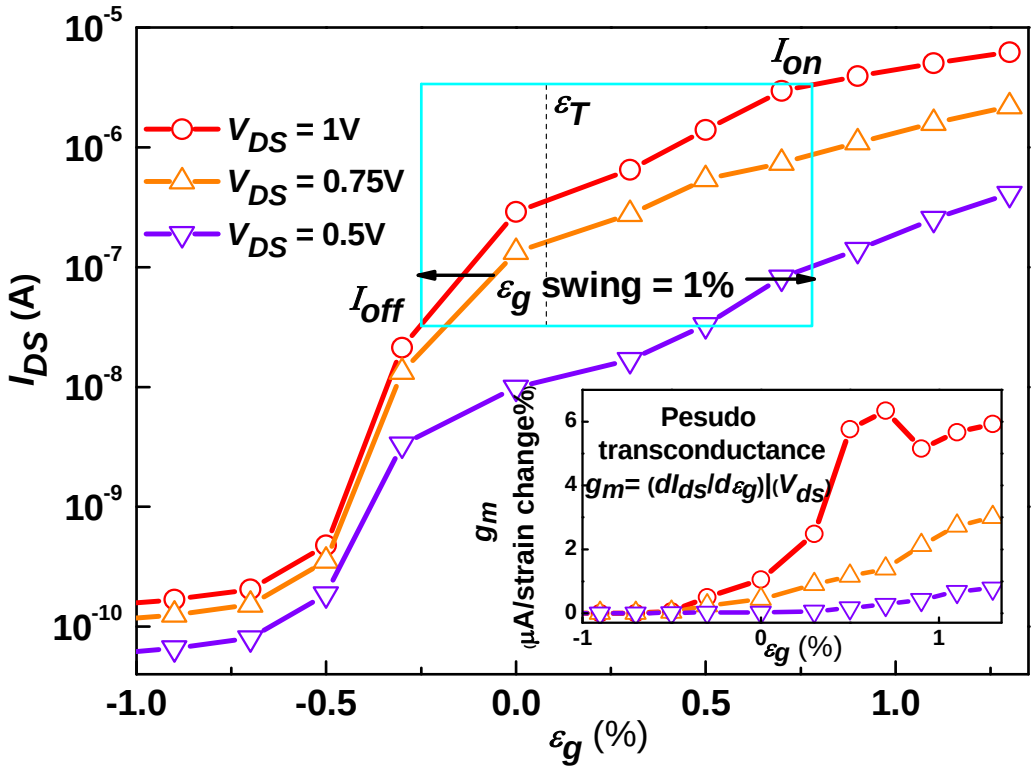

Fig. S1. $I_{ds} - \varepsilon_g$ transfer characteristic for ZnO NW SGT. $I_{DS} - \varepsilon_g$ transfer characteristic for the ZnO SGT device under three different V_{DS} bias values: 1 V, 0.75 V and 0.5 V, respectively. The blue square defines the 1% gate strain window. On and off currents are defined as the values obtained at $\varepsilon_{g\ (off)} = \varepsilon_T$ - 0.3% and $\varepsilon_{g\ (on)} = \varepsilon_T$ + 0.7%, so that 70% of the ε_g swing above the threshold strain ε_T turns the ZnO NW SGT on, while the remaining 30% defines the "off" operation range. (Inset) Pseudo transconductance for this ZnO NW SGT with V_{DS} bias values of 1 V, 0.75 V and 0.5 V, respectively, from top to bottom.

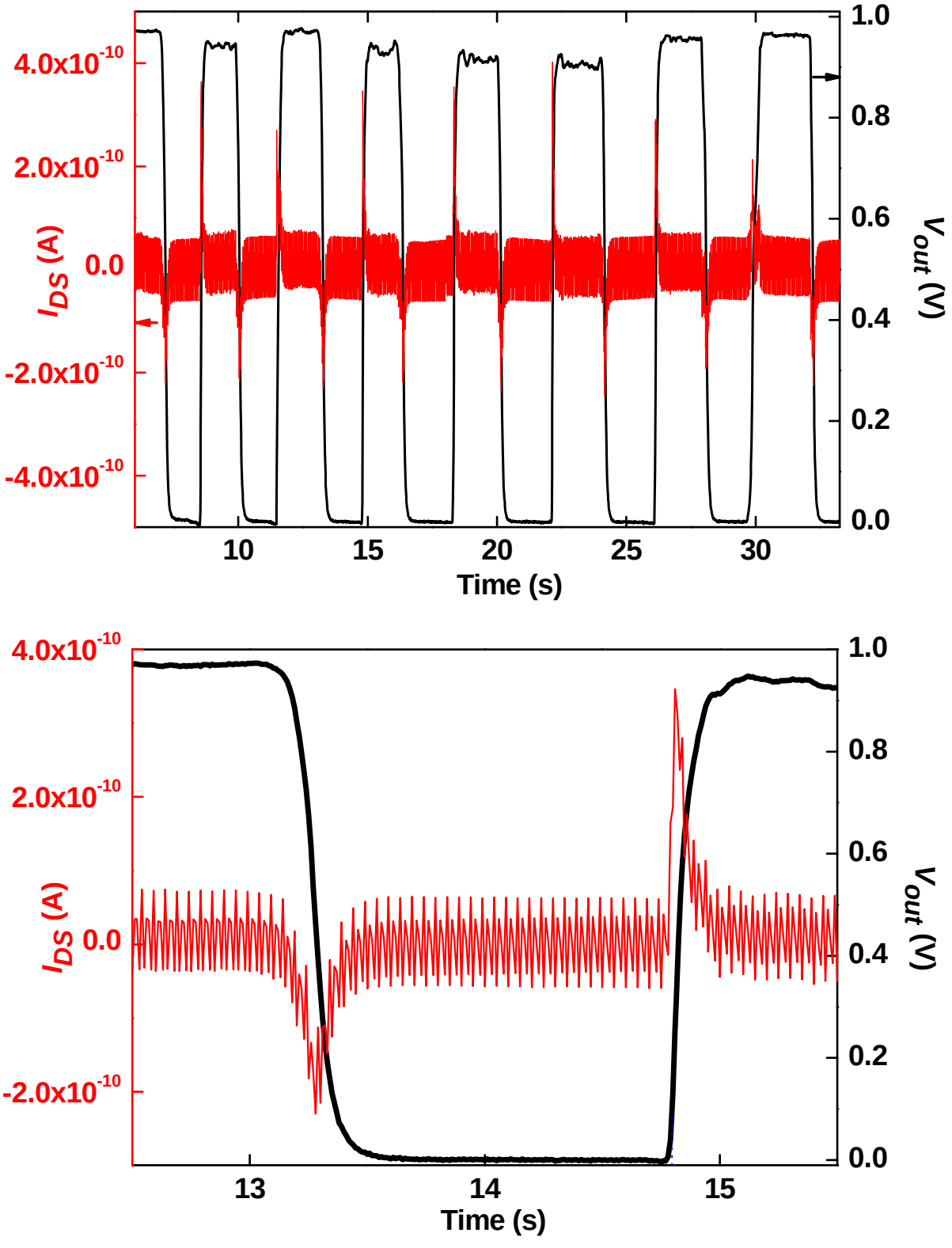
4.0x10-10
2.0x10-10
0.0
-2.0x10-10
-4.0x10-10
IDS (A)
1.0
0.8
0.6
0.4
0.2
0.0
Vout (V)
10
15
20
25
30
Time (s)
4.0x10-10
2.0x10-10
0.0
-2.0x10-10
IDS (A)
1.0
0.8
0.6
0.4
0.2
0.0
Vout (V)
13
14
15
Time (s)

Fig. S2. Temporal characteristics of current and voltage on a typical ZnO-NW SGI. One of the possible power dissipation sources in ZnO-NW SGIs, direct path short-circuit current, I_{dp}, occurs due to the finite slope of the input strain signal, which causes a direct current path between V_{DD} and GND for a short period of time during switching when both the ZnO-NW SGTs in a SGI are on. The absolute charges for the two current spikes in the magnified part are $1.99\times10^{-11}C$ (negative spike) and $2.97\times10^{-11}C$ (positive spike), respectively. It is proposed that the current spikes observed result from the superposition of the currents generated by the piezoelectric ZnO NWs (s4) and the dynamic direct path short-circuit current I_{dp}. The current spikes resulted from current generating process in the NWs can be negative or positive here depending the sign of straining rate, while the spikes of I_{dp} should be all positive. Therefore, I_{dp} can be determined as around 50 pA using simple superposition calculation.

	“0 0” ⇄ “1 1”		“0 1” ⇄ “1 1”		“1 0” ⇄ “1 1”	
SGT 1	**On**	**Off**	**On**	**Off**	**Off**	**Off**
SGT 2	**Off**	**On**	**Off**	**On**	**On**	**On**
SGT 3	**Off**	**On**	**On**	**On**	**Off**	**On**
SGT 4	**On**	**Off**	**Off**	**Off**	**On**	**Off**

Table S1. Two kinds of transitions occur during the switching of a ZnO NW strain gated NAND gate. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of Table S1 (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of Table S1 (with blueish color). The two numbers in the quotation marks represent the logic levels for strain inputs on the SGIs in a ZnO NW strain gated NAND gate.

	“0 0” ⇄ “1 1”		“0 0” ⇄ “1 0”		“0 0” ⇄ “0 1”	
SGT 5	**Off**	**On**	**Off**	**On**	**Off**	**Off**
SGT 6	**On**	**Off**	**On**	**Off**	**On**	**On**
SGT 7	**On**	**Off**	**On**	**On**	**On**	**Off**
SGT 8	**Off**	**On**	**Off**	**Off**	**Off**	**On**

Table S2. Two kinds of transitions occur during the switching of a ZnO NW strain gated NOR gate. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of Table S2 (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of Table S2 (with blueish color). The two numbers in the quotation marks represent the logic levels for strain inputs on the SGIs in a ZnO NW strain gated NOR gate.

1. References and notes

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