Piezoelectric nanogenerator using CdS nanowires

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Vertically grown cadmium sulfide (CdS) nanowire (NW) arrays were prepared using two different processes: hydrothermal and physical vapor deposition (PVD). The NWs obtained from the hydrothermal process were composed of alternating hexagonal wurtzite (WZ) and cubic zinc blende (ZB) phases with growth direction along WZ ⟨0001⟩ and ZB [111]. The NWs produced by PVD process are single crystalline WZ phase with growth direction along ⟨0001⟩. These vertically grown CdS NW arrays have been used to converting mechanical energy into electricity following a developed procedure [Z. L. Wang and J. Song Science **312**, 242 (2006)]. The basic principle of the CdS NW nanogenerator relies on the coupled piezoelectric and semiconducting properties of CdS, and the data fully support the mechanism previously proposed for ZnO NW nanogenerators and nanopiezotronics. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2831901]

CdS is a piezoelectric semiconducting material[1] with an energy band gap of about 2.5 eV. A wide range of applications have been demonstrated for one-dimensional CdS nanostructures, such as waveguide,[2] photoconductor,[3] logic gate,[4] and field emiter.[5] In recent years, applications of CdS nanorods and thin films in energy conversion, for example, dye sensitized solar cells[6] and thermoelectronics,[7] have attracted increasing research interests, respectively. These developments aim at extracting and conserving energy from environment by exploring the semiconducting properties of the CdS nanostructures.

Recently, ZnO nanowire (NW) arrays based nanogenerators were demonstrated for converting mechanical energy to electricity by utilizing the coupling effects of the semiconducting and piezoelectric properties of ZnO.[8–10] In this paper, we demonstrate that CdS NWs can also be used for converting mechanical energy into electricity. Our results not only fully support the mechanism previously proposed for the ZnO NW nanogenerators but also show that CdS is a promising candidate for future nanoscale power devices.

Vertically CdS NW arrays were grown by two different approaches: hydrothermal and physical vapor deposition (PVD). The hydrothermal process followed the procedures of reported in literature with minor modifications.[11] Cd foils and thiosemicarbazide were used as the Cd and S sources at a molar ratio of 3:2. An amount of 5 ml de-ionized water was first added into a Teflon-lined vessel of 25 ml capacity, and then ethylenediamine was added into the same vessel to reach 80% capacity of the vessel. The reaction was carried out at 180 °C for 20 h. As for the PVD approach, CdS powders and Au coated Si(111) wafer were used as the CdS source and collecting substrate, respectively. The temperature and pressure of the deposition chamber were set at 950 °C and 160 torr, respectively. Argon gas of 50 SCCM (SCCM denotes cubic centimeter per minute at STP) was used to carry the CdS vapors to the downstream of the growth chamber for deposition. The deposition was ran for 30 min at the peak temperature.

The morphology of the hydrothermally grown CdS NWs was characterized with scanning electron microscope (SEM). As shown in Fig. 1(a), these NWs were 150 nm in diameter and several micrometers in length. The x-ray diffraction (XRD) pattern of the as-grown CdS NWs was shown in Fig. 1(b). Also included in Fig. 1(b) are the XRD patterns of the reference cubic zinc blende[12] (ZB) and hexagonal wurtzite[13] (WZ) phases of CdS crystals for comparison purposes. All of the diffraction peaks, except the one located at 26.4°, can be indexed to the WZ phase. The diffraction peak at 2θ of 26.4° is a combined contribution from WZ (0002) and ZB (111) planes. The coexistence of the two phases can be clearly seen from the high-resolution transmission electron microscopy (HRTEM) image shown in Fig. 1(d). The NW is composed of alternating ZB and WZ phases, with alternating atomic layer stacking sequence from *ABC* to *AB* along the growth direction of the NWs. The growth direction was identified to be along ZB [111] and WZ ⟨0001⟩. The streaks appearing in the corresponding selected area electron diffraction (SAED) pattern were a direct result of the stacking faults resulting from the phase transformation between ZB (ABC) and WZ (AB).

Piezoelectric measurements were performed in contact mode of an atomic force microscope (AFM) using a Pt coated Si tip with a cone angle of 70°.[8] The cantilever had a spring constant of 1 N/m. In AFM contact mode, a constant normal force of 5 nN and a scanning speed of 150.24 μm/s were maintained between the tip and sample surface. By scanning the tip across the sample [Fig. 2(a)], output voltage was detected across an external load.

The process for generating the electric current can be derived from a detailed analysis of the output voltage peak and the topological profile received by the tip when scanned across a NW. During the tip scans, no voltage output signals were observed if the tip touched only the stretched side of the NW and did not lift up to go beyond the central line of the NW to reach the compressed side. A negative voltage output signal was detected when the tip went beyond the NW to reach the compressed side of the NW, as shown in the topography (red curve) and output voltage (blue curve) images of Fig. 2(b). This is clearly indicated by a delayed out-

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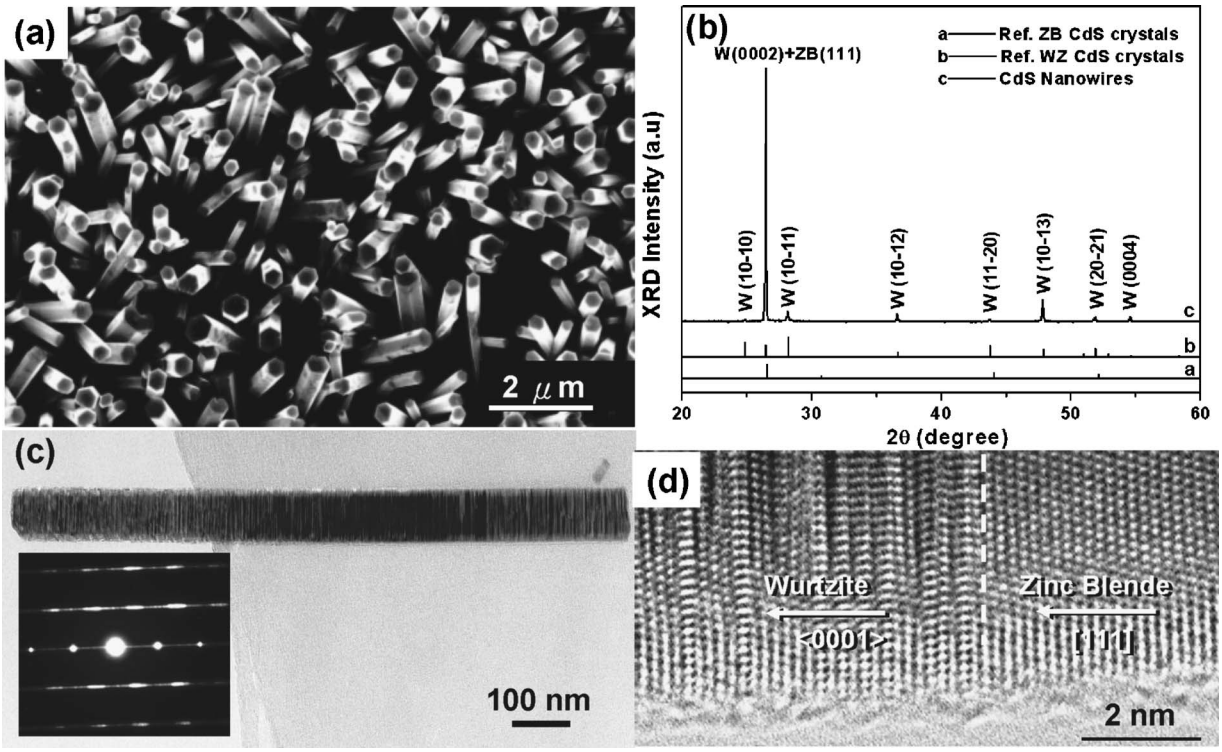

FIG. 1. [(a) and (b)] Top view SEM image and XRD pattern of the CdS nanowires prepared from the hydrothermal process, respectively. (c) TEM image of a single CdS nanowire. The inset is the corresponding SAED pattern. (d) HRTEM image of a single CdS nanowire.

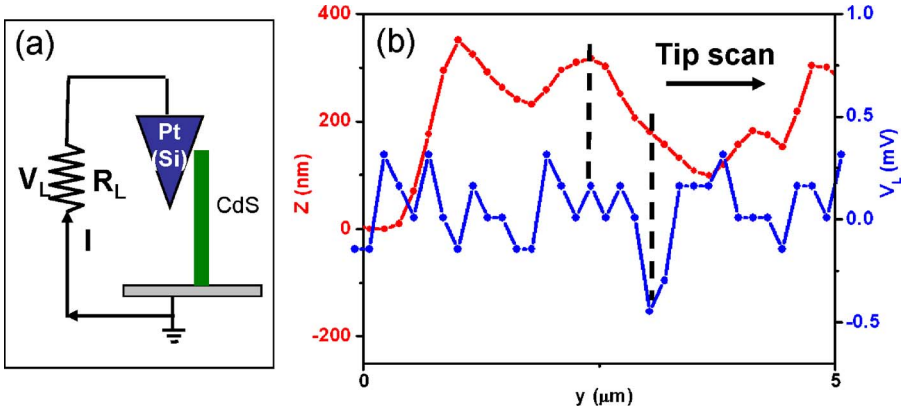

FIG. 2. (Color online) (a) Schematic of the AFM measurement system. (b) Line profiles of topography (red) and output voltage (blue) scanned across CdS nanowires.

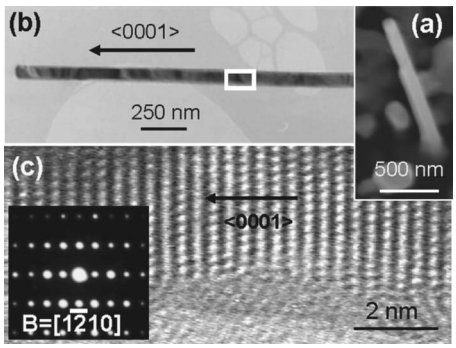

FIG. 3. [(a) and (b)] Side view SEM and TEM images of a single CdS nanowire produced from the PVD process. (c) HRTEM image of a single CdS nanowire at the marked region of (b). The inset is the corresponding SAED pattern of the nanowire recorded from the marked region in (b).

put in voltage signal in reference to the surface profile image of the NW. The typical magnitude of the output voltage was $\sim -(0.5-1)$ mV, where the negative sign means that the generated current flowed from the tip to the NW. The low voltage output is likely to be resulted from the phase transition between ZB and WZ phases along the growth direction of the NW, because WZ phase is piezoactive, while ZB phase is not.[14] The presence of the ZB phase along the growth direction is disadvantageous to the piezoelectronic performance of the CdS NWs.

To improve the voltage output using solely the WZ phase, CdS NW arrays were prepared using a PVD process at a much higher temperature of 950 °C. The as-grown NWs are about 100 nm in diameter and over 1 μm in length, as shown in the EM images of Figs. 3(a) and 3(b). The dot pattern of SAED shown in the inset of Fig. 3(c) reveals the single crystalline WZ phase of the NW. The HRTEM image of Fig. 3(c) reveals the NW grew along the ⟨0001⟩ direction.

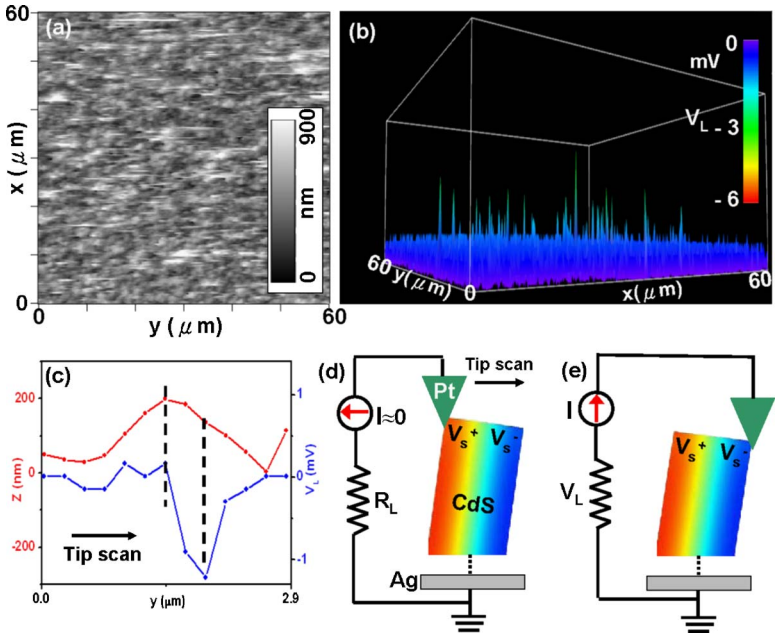

FIG. 4. (Color online) [(a) and (b)] The topography and corresponding voltage output images of the nanowire arrays prepared from the PVD process, respectively. (c) Line profiles of topography (red) and output voltage (blue) scanned across CdS nanowires. [(d) and (e)] Contact between the AFM tip and a semiconductor CdS nanowire at two reversed local contact potentials (positive and negative), showing reverse- and forward-biased Schottky rectifying behavior, respectively. The process in (d) is to generate and preserve the charges/potential, and the process in (e) is to discharge the potential through a flow of electrons from the circuit under the driving of the piezoelectric potential.

Furthermore, there was no trace of the presence of the ZB phase in the NW.

The topography [Fig. 4(a)] and corresponding output voltage [Fig. 4(b)] images across the load were recorded simultaneously when the AFM tip scanned over the NW arrays. The magnitude of the voltage output is around −3 mV, much larger than that from the NW arrays produced with the hydrothermal process. Evidently, the pure WZ phase of the NWs from the PVD process gave higher voltage outputs.

The mechanism proposed previously for the ZnO NW based nanogenerators applies for the present case.[8,10] The electron affinity of *n*-type CdS is 4.8 eV,[15] while the work function of Pt is about 6.1 eV. There would be a Schottky barrier formed at the Pt-CdS contact. In Fig. 4(d), as the AFM tip started to deflect the NW, a positive potential ($V_s^+ > 0$) was produced at the stretched side of the NW, while a negative potential ($V_s^- < 0$) was induced at the compressed side.[8] The potential of Pt metal tip is near zero, $V_m = 0$. No voltage signals were observed due to the presence of the reverse-biased Schottky barrier contact between the Pt tip and the stretched side of the *n*-type CdS NW ($\Delta V = V_m - V_s^+ < 0$). Figure 4(d) demonstrates the charge/potential accumulation process by bending a CdS NW. When the AFM tip went beyond the central line of the NW and reached the compressed side, as shown in Fig. 4(e), negative voltage signals were produced because of the presence of the forward-biased Schottky barrier contact between the Pt tip and the compressed side of the CdS NW ($\Delta V = V_m - V_s^- > 0$). Figure 4(e) shows how the charges/potentials were released from the NW. The topography (red) and voltage output (blue) images of Fig. 4(c) provide clear evidence for the above discussed charge accumulation and release processes when bending a CdS NW.

In conclusion, CdS NW based piezoelectric nanogenerators were demonstrated. The Schottky barrier formed at the Pt-CdS contact is responsible for the charge accumulation and release processes. The proposed model is entirely consistent to that proposed for the ZnO NW based nanogenerators and nanopiezotronics.[16]

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