Bridged ZnO nanowires across trenched electrodes

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Using a hydrothermal synthesis approach, large scale and laterally bridged nanowires have been grown across trenched Au/Si, Au/SiO_2/Si, and ZnO/Si electrodes. This technique shows a low temperature (80 °C) approach for growing ZnO nanowires on a prepatterned substrate, showing its potential for integrating with silicon based technology. The *I-V* characteristics of the nanowires have been measured and their nonlinear behavior has been analyzed. It is suggested that the nonlinear behavior might be due to the dominant phonon scattering and the impurity involved grain boundaries in the multinanowire bridges. The bridged nanowire arrays could be useful for fabricating gas, chemical, or biochemical nanosensor arrays. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2794417]

Integration of individual nanowire (NW) or nanotube devices into a large-scale nanosystem in a precise and efficient way has been an attractive research area. It remains a big challenge despite fast development of nanofabrication and manipulation techniques.[1,2] Using as-grown NWs as building blocks, previous work has demonstrated that cross-bar arrays of GaP, InP, and Si NWs can be fabricated using flow field and electrical field induced self-assembly.[3–5] The challenge for this type of assembly is scale up and precise control over the self-assembly.

Seeking an alternate strategy that can directly grow NWs onto prefabricated nanodevice structures is of great interest. Some recent successes have shed some light. For example, using metal-organic chemical vapor deposition, an individual Si NW has been grown as a bridge across a microscale trench on a Si or silicon on insulator substrate.[6,7] Using a layer with ZnO seeds, lateral growth of ZnO NWs across a Si trench via a vapor-solid method was also realized.[8,9] However, the required high temperature in the vapor-phase deposition undoubtedly limits their application for low temperature substrates such as plastic substrates and annealing-sensitive platforms. To solve this problem, a hydrothermal synthesis method[10–12] has been used in this work to synthesize similar structures but at a much lower temperature (80 °C). Large-scale and laterally bridged ZnO NWs have been grown across Au electrode arrays with separations of 500 nm and 10 μm. The as-bridged NW diameters range from 50 to 1000 nm depending on the growth conditions. Using a four-terminal approach, current-voltage characteristics of the grown structures have been characterized at both room temperature (295 K) and low temperature (77 K).

The growth of ZnO NWs was conducted by suspending substrates that had been modified with Au or ZnO seeds in a Pyrex glass bottle filled with an equal molar aqueous solution of zinc nitrate hydrate [$Zn(NO_3)_2 6H_2O$, Fluka, ≥99.0% (KT), 0.01*M*] and hexamethylenetetramine ($C_6H_{12}N_4$, Fluka, 0.01*M*) at 80 °C. The reaction time was 1–4 h for both substrates coated with Au or ZnO seeds. After reaction, the substrates were removed from the solution, rinsed with deionized water, and then dried in air at 65 °C overnight.

Figure 1 shows a schematic diagram of the synthesis strategy. To define Au side wall electrodes across trenches with 10 μm separation, typical photolithography, dry etching, and Bosch processes were used. The process starts with depositing 100 nm of SiO_2 on a 4 in. silicon wafer (*p* type, ⟨100⟩, 0.01 Ω cm) [Fig. 1(a)] using uniaxis plasma enhanced physical vapor deposition. A typical lithography process was then applied to the wafer with AZ5214 image reversal photoresist. The pattern was subsequently transferred to the SiO_2 via dry etching using a Plasma-Therm inductive coupled plasma (ICP) etcher. A Bosch process was utilized to form the deep (etched-through) trenches using ICP with the SiO_2 acting as the hard mask. After that, a 100 nm thick Au coating was deposited on the entire wafer, including the side walls and bottoms of the trenches, using a CVC dc sputterer. Finally, the SiO_2 layer and the Au coating on top of it were

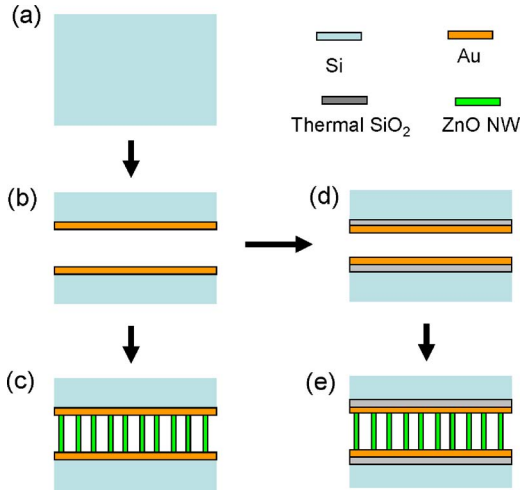

FIG. 1. (Color online) Fabrication and growth processes for growing bridged nanowires across trenched electrodes.

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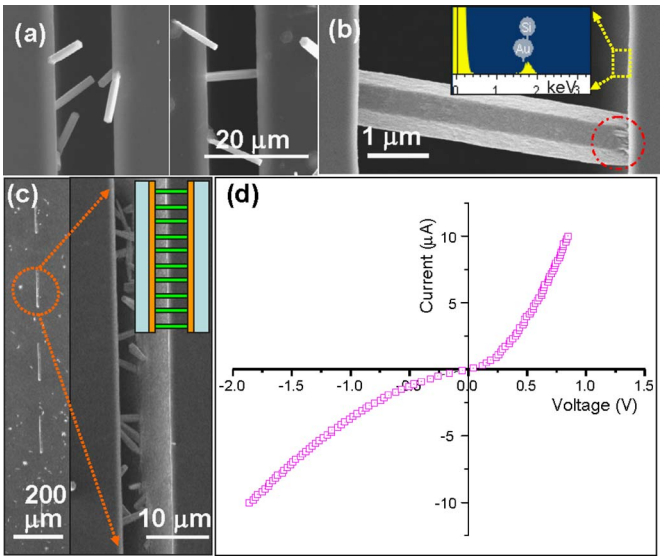

FIG. 2. (Color online) A set of SEM images [(a)–(c)] showing various configurations of as-grown nanowire arrays bridging across Au/Si electrodes and (d) the corresponding nonlinear and asymmetric current-voltage characteristics.

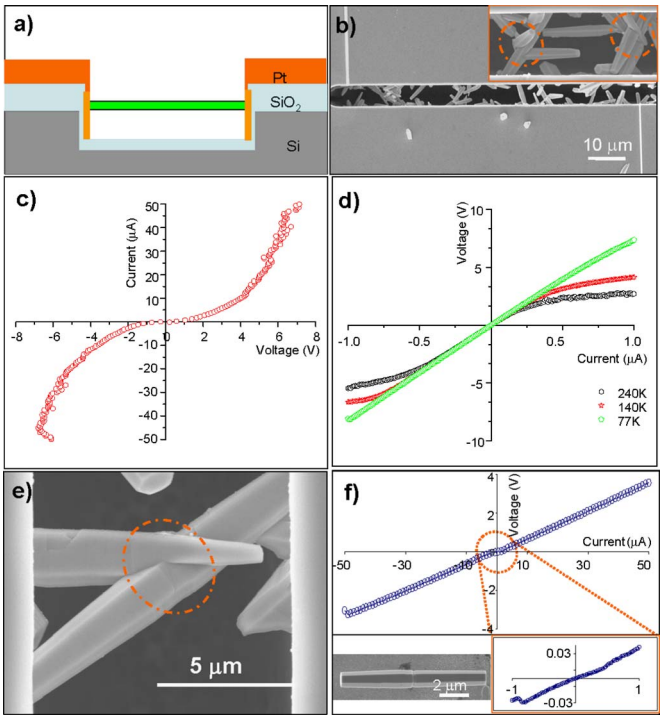

FIG. 3. (Color online) (a) Schematic for the transport measurement. (b) SEM image of the bridged nanowire array. (c) and (d) are, respectively, the room temperature and low temperature *I-V* curves for the nanowire arrays across $Au/SiO_2/Si$ electrodes. (e) and (f) are, respectively, a typical multinanowire bridge grown with interfacial grain boundaries and the corresponding nonlinear *I-V* characteristics of a freestanding twin-type nanowire with one grain boundary.

lifted off in HF. After this process, the Au/Si side wall electrodes were formed across the 10 μm trench [Fig. 1(b)]. The process of steps b and c represents a fabrication process to form a nanowire device array across the microtrenches on Si substrate. An additional 50 nm thermal oxide is formed on the Au/Si substrates by virtue of thermal oxidation in steps b–d. During the processing, caution needs to be taken to avoid short circuits between the paired side wall Au electrodes.

Figure 2 is a set of scanning electron microscopy (SEM) images and *I-V* characterization of the as-grown NW devices on the Si substrate. The left part of Fig. 2(a) shows the NWs selectively grown from both side wall Au electrodes at 10 μm separation, but without touching the opposite side walls. As growth time increased, nanowires grew longer and eventually touched the opposite side wall [right side of Fig. 2(b)]. The wire diameter is around 2 μm with a defined length of 10 μm. From the magnified SEM image in Fig. 2(b), the wire grew from right-hand side wall to the left-hand side wall, as shown by the rooted region indicated by the red dotted circle on the right-hand side. An inset energy dispersive spectroscopy spectrum from the side wall revealed the composition of the Au layer on Si side wall. Figure 2(c) displays well aligned NWs that bridge across a 10 μm wide microtrench.

A four-terminal electrical measurement was conducted across a pair of side-wall Au electrodes. For electrical characterization, a Keithley 6221 ac/dc current source and 2182A nanovoltmeter combination was used for four-terminal current-voltage measurements. For both room and low temperature characterizations, a VPF-700 LN2 optical cryostage was used as a vacuum chamber to hold the NW devices. Au wire bonding and focused ion beam (FIB) nanolithography were used for ensuring good contact and interconnects between the nanowire device and the test platform.

As shown in Fig. 2(d), the electrical measurement gave rise to *p-n* junctionlike nonlinear current-voltage characteristics. At forward bias, the degree of nonlinearity is larger than that at reverse bias, resulting in an asymmetric *I-V* characteristic. At a low current range of ±1 μA, the *I-V* characteristic was almost linear, and the resistance was about 500 kΩ. When the source current increases to ±10 μA, the degree of nonlinearity became significant. At large forward bias, the resistance is close to 100 kΩ, while at high reverse bias, the resistance is around 200 kΩ. Over ten such devices have been tested, displaying consistent asymmetric nonlinear *I-V* characteristics. This asymmetric *I-V* behavior might be due to possible asymmetric contacts across the Au/Si electrode pair, resulted from the junctions formed between the FIB deposited Pt leads and the *p*-type Si substrate.[8,9]

When the NWs bridged across the Au electrodes on SiO_2 (50 nm)/Si substrates, having an intermediate silicon oxide layer of approximately the same thickness as the Au coating reduces the contact effect between the Pt interconnect/Si substrate junction. Figure 3(a) is a schematic circuit with a SiO_2 insulation layer on the Si substrate. A real device structure is shown next to the schematic diagram with an array of bridged NWs. The two vertical lines at the top left-hand side and bottom right-hand side are 200 nm Pt interconnects deposited using focused ion beam microscopy.

Figure 3(b) is an *I-V* curve measured at room temperature and is observed to be rather symmetric. At a low current range of ±1 μA, the resistance is ~8 MΩ, an order of magnitude larger than that of devices described in Fig. 2, suggesting a drastic reduction of current leakage due to the existence of an intermediate SiO_2 insulation layer between Au/Pt interconnects and the Si substrate. When the current was increased to ±10 μA, the resistance at higher bias was close to 400 kΩ. The degree of nonlinearity is about 20. Figure 3(c) shows low temperature electrical characteristics at a low bias range of ±1 μA. When the temperature de-

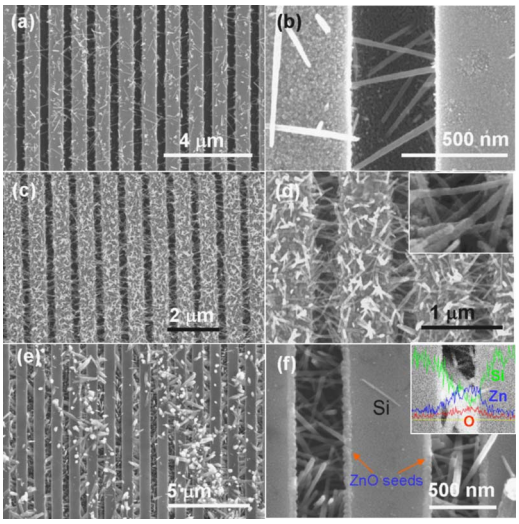

FIG. 4. (Color online) Bridged ZnO nanowire arrays across a 500 nm nanotrench array with different densities, where (a) and (b) are the most sparse ones, (c) and (d) are the dense ones, and (e) and (f) are the dense ones after removal of the ZnO NWs on the top of the trenches.

creased from 240 to 77 K, it was evident that the degree of nonlinearity decreased as well. At 77 K, the *I-V* behavior was linear. This result suggests that the nonlinear electrical behavior of ZnO nanowire at room temperature is likely due to domination by phonon scattering. Another six bridged NW devices across $Au/SiO_2/Si$ electrodes have also been tested, which have yielded similar *I-V* characteristics as the above described one, suggesting a good reproducibility of the as-grown NW devices.

It is worth noting, in addition to the temperature effect, that the possible microscopic factor leading to the *varistor-like* nonlinear *I-V* behavior could be the existence of frequent multiple grain boundaries between the crossed NWs in the bridges shown in Figs 3(b) and 3(d), indicated by the orange highlighted dotted circle. To confirm this possibility, a typical electrical measurement was conducted on a hydrothermal grown twin nanowire with a grain boundary [inset of Fig. 3(e)]. The *I-V* characteristics were found to be nonlinear as the dotted circle indicated in Fig. 3(e) and clearly described in the bottom right inset. With considering the tiny amount of impurities such as Co, Cd, Ni, and Fe present in the $\geqslant 99\%$ $Zn(NO_3)_2 \cdot 6H_2O$ precursor, it is still likely some impurities segregate at the NW grain boundaries. This would result in the varistorlike nonlinear *I-V* characteristics by forming electrostatic potential barriers across the multigrain boundaries.[13–16]

Further, using ZnO seeds as electrodes, large scale well-aligned array of NW bridges have been grown. Figure 4 is a set of SEM images showing horizontally aligned nanowires across the nanotrench arrays. The width of each trench is about 500 nm. In Figs. 4(a) and 4(b), sparsely grown ZnO NWs ran across each nanotrench, forming a network of horizontal nanowire bridges. These NWs have a uniform diameter of ~50 nm. As the growth time increased, the densities of the NW networks became higher, as indicated in Figs. 4(c) and 4(d). The frequency of crossed nanowires is low [Fig. 4(d)].

The access nanowires on the top surface of the trenches can be removed by sweeping across the surface of the substrate. Figure 4(e) is a SEM image displaying the cleaned substrate surface. Figure 4(f) is a magnified SEM image showing the densely packed nanowire bridges embedded in two nanotrenches. A layer of ~50 nm ZnO seeds can be seen as indicated by the orange arrowheads.

In summary, using low temperature hydrothermal synthesis, large scale and laterally bridged NWs have been grown across trenched Au/Si, Au/SiO2/Si, and ZnO/Si electrodes. The technique shows a low temperature (80 °C) approach for growing ZnO NWs on a prepatterned substrate. *I-V* characteristics of the NWs have been measured and their non linear behavior has been analyzed. The bridged nanowire arrays could be useful for fabricating gas, chemical, or biochemical nanosensor arrays.

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