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Full paper

Mechano-driven logic-in-memory with neuromorphic triboelectric charge-trapping transistor☆

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ABSTRACT

In the post-Moore's Law era, there is a growing trend towards the development of advanced electronic devices that combine sensory perception, data storage, and computation for various applications. Two-dimensional semiconductor transistors, which utilize charge storage mechanisms, present a promising avenue for future information devices. Here, we introduce a neuromorphic triboelectric charge-trapping $MoTe_2$ transistor with stacked high-*k* dielectric structure, aiming to facilitate mechano-driven logic-in-memory for neuromorphic computation. By gating through triboelectric potential, the device demonstrates superior electrical performance, including an impressive switching ratio (>10^5), minimal off-state current (~0.6 pA), and robust cyclic stability. By modulating the trapped charges in the stack gate structure via tribopotential modulation, the conductivity state of the $MoTe_2$ channel can be readily controlled, realizing an exceptional mechano-driven nonvolatile memory with a retention time of up to 10^4 seconds, consistent switching behavior over 100 cycles, and multi-level data storage capabilities at 8 levels. Furthermore, a mechano-driven programmable inverter can be achieved by connecting a load resistor in series. The triboelectric charge-trapping transistor also possesses the capacity to emulate typical synaptic characteristics at low energy levels (~147 fJ). Leveraging the finely tunable conductivity through tribopotential, we demonstrate a mechano-assisted artificial neural network capable of recognizing handwritten digits with an accuracy rate of approximately 88.59%. These findings underscore the significant potential of the triboelectric charge-trapping transistor in mechanical-assisted real-time interaction, energy-efficient data storage, and neuromorphic computing.

1. Introduction

With the rapid development of artificial intelligence and Internet of Things (IoTs), the increasing demand for high-density data collection scenarios necessitates more advanced and intelligent sensing networks to achieve efficient and low-energy process for data acquisition.[1,2] In

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traditional integrated circuits, the physical separation between sensing, storage, and computing units requires additional signal encoding/decoding for data transfer between these units, leading to the complexity of information processing, high energy consumption, and risky bottlenecks and delays.[3–5] To overcome the limitations of traditional architecture, a promising solution is to break the boundaries between computing modules and storage units by integrating these functionalities into one single structure through the brain-inspired in-memory computing technology.[6–8] This emerging architecture allows parallel information processing and storage, and significantly enhance the capability and efficiency of handling high-density data streams.[9–12] The in-memory computing technology has shown great promise in accelerating specific applications in machine learning and artificial intelligence.[2,13,14] However, most reported in-memory computing devices lack effective sensation and interaction strategies.

The booming triboelectric nanogenerator (TENG) offers a killer technology for harvesting low-frequency and high-entropy energy, which utilizes the effects of electrostatic induction and triboelectrification to convert mechanical energy generated from environmental vibrations or movements into electricity.[15–18] In certain scenarios, these vibrations or movements are also associated with some physical variables to be monitored, such as displacement, pressure, or strain. Hence, TENG not only serves as a power source but also possesses sensing capabilities with high sensitivity, fast response, and excellent stability,[16,19] which makes it widely used in micro-nano energy source[20–28], self-powered sensation[29–34], high-voltage power supplies[35–38], and blue energy fields[39–41]. Integrating TENG with logic devices or neuromorphic memory enables the construction of an advanced intelligent sensing device with integrated perception, storage, and computing functionalities, achieving the prototype of sensing-memory-computation integration.[24,27,42–45] This device significantly simplifies the transmission process, reduces hardware volume, boasts high response speed, and greatly lowers energy dissipation. Notably, the coupling effect between the externally stimulated tribopotential and semiconductor transport characteristics establishes a direct and active correlation between the external environment and output signals.[46–49] This event-triggered interaction mechanism exhibits good adaptability and high efficiency, which is more suitable for complex and changeable external environments.[48,50,51] In addition, logic devices and artificial synapses based on tribotronic transistors have drawn widespread attention and validated various functional devices.[49,51] Among these devices, two-dimensional (2D) semiconductor devices are the primary research focus due to their tunable band structure, excellent optoelectronic properties, and high electron mobility. For instance, the tribotronic floating-gate MoS_2 transistor achieves multiple synaptic plasticity through mechanical displacement and is successfully used to construct an ANN for mechanoplastic neuromorphic logic switches and data storage.[24] Besides, utilizing tribopotential modulation on the InSe/h-BN/graphene stack is also possible to achieve quasi-nonvolatile and synaptic characteristics through mechanical behavior, featuring low-power consuming and mechanical writing/reading capability.[45] Using semi-floating-gate design, a multifunctional tribotronic WSe_2/h-BN/graphene transistor with reconfigurable p-n junctions and artificial synapses is also developed.[44] Moreover, an artificial synapse based on graphene/MoS_2 heterostructure exhibits mechano-photonic bimodal plasticity and has potential applications in general ANN and mixed neuromorphic computing.[26] Despite obtaining unusual electronic characteristics, currently reported triboelectric logic circuits and artificial synapse devices still suffer from poor stability and short retention time, remaining significant challenges for scientific research and commercialization (Table S1).

In this work, we present a mechano-driven logic-in-memory device based on triboelectric charge-trapping transistor with stacked gate structure, which can be programmed by mechanical behavior and implemented for mechano-driven logic gate and neuromorphic computation. The triboelectric charge-trapping transistor consists of a contact-separation TENG unit and a $MoTe_2$ transistor with stacked gate dielectrics, unifying the functionality of non-volatile memory, logic gate, and neuromorphic computation mediated by mechanical behavior (i.e., mechano-driven logic-in-memory). Upon the mechanical displacement of the integrated TENG unit, the triboelectric charges mediated tribopotential (V_{TENG}) can effectively modulate the charge-trapping $MoTe_2$ transistor via the stack dielectrics, which allow the semiconductor charge carriers (electrons or holes) to tunnel through the Al_2O_3 barrier layer and store in the HfO_2 charge-trapping layer. The triboelectric charge-trapping $MoTe_2$ transistor exhibits excellent mechanical behavior derived electrical properties of high switching ratio ($>10^5$), low off-state current (approximately 0.6 pA), and good cycling stability. Additionally, it possesses remarkable mechano-driven memory characteristics, including a program/erase current ratio exceeding 3×10^2, retention time of up to 10^4 seconds, 8-level multibit data storage capability, over 100-switching cyclic durability, and stable operation maintained for up to three months. Relying on the excellent memory properties, a mechano-programmable resistor-loaded inverter is also available to implement logic state switching by programming channel conductivity with TENG displacement. Moreover, a mechanoplastic artificial synapse at femtojoule ($\sim$147 fJ) is emulated with essential synaptic functions based on the triboelectric charge-trapping transistor. Prominent synaptic behaviors, including excitatory post-synaptic currents (EPSC), paired-pulse facilitation (PPF), short-term memory (STM), long-term memory (LTM), and learning-forgetting-relearning behaviors are successfully simulated under mechanical displacement pulse. The achieved dynamic updating of synaptic weights by spatiotemporal mechanical information establishes the foundation for the application of triboelectric charge-trapping transistors in the field of mechano-driven neuromorphic computing. Based on this, we have successfully constructed an ANN with three-layer perceptron for pattern recognition, achieving an accuracy rate of $\sim$88.59% in recognizing handwritten digits using the Modified National Institute of Standards and Technology (MNIST) dataset. The demonstrated mechano-driven logic-in-memory based on triboelectric charge-trapping transistor provides a facile and sophisticated configuration for data storage, logic gate, and next-generation neuromorphic computing, holding significant importance in advanced artificial intelligence and interactive neural interfaces.

2. Results and discussion

Fig. 1a illustrates the schematic structure of the mechano-driven logic-in-memory device based on triboelectric charge-trapping transistor in stacked gate design and driven by the integrated TENG unit, which is endowed with the mechanical behavior derived nonvolatile memory, logic operation, and biomimetic synaptic functions (Fig. 1b). In the neuromorphic triboelectric charge-trapping transistor, mechanically exfoliated $MoTe_2$ flake is utilized as the semiconductor channel due to its relatively weak Fermi level pinning at the contact interface and small bandgap for efficient band modulation and control of carrier polarity through various methods. Thermal-deposited Cr/Au (7/20 nm) are defined as source-drain electrodes through standard electron beam lithography (EBL) and lift-off processes; the essential control-gate adopts a high-k gate dielectric stack structure of $Al_2O_3/HfO_2/Al_2O_3$ consecutively deposited by atomic layer deposition (ALD). Cross-sectional transmission electron microscope (TEM) image of the stacked gate device provides a clear view of the precise layer-to-layer stacking structure (Fig. 1c), in which the actual thickness of the stacked gate dielectrics matches the theoretical value of 7/8/25 nm and the thickness of $MoTe_2$ channel is estimated to be approximately 8.5 nm ($\sim$10 layers, consistent with the atomic force microscopy result in Figure S1) with an interlayer spacing of $\sim$0.79 nm (Fig. 1d, belongs to 2 H-$MoTe_2$ crystalline structure and further confirmed by confocal Raman spectroscopy in Fig. 1e).[52,53] The TENG unit composed of a sandwiched structure of Cu/polytetrafluoroethylene (PTFE)/Cu in contact-separation mode is integrated to supply the tribopotential to power the transistor and implement the

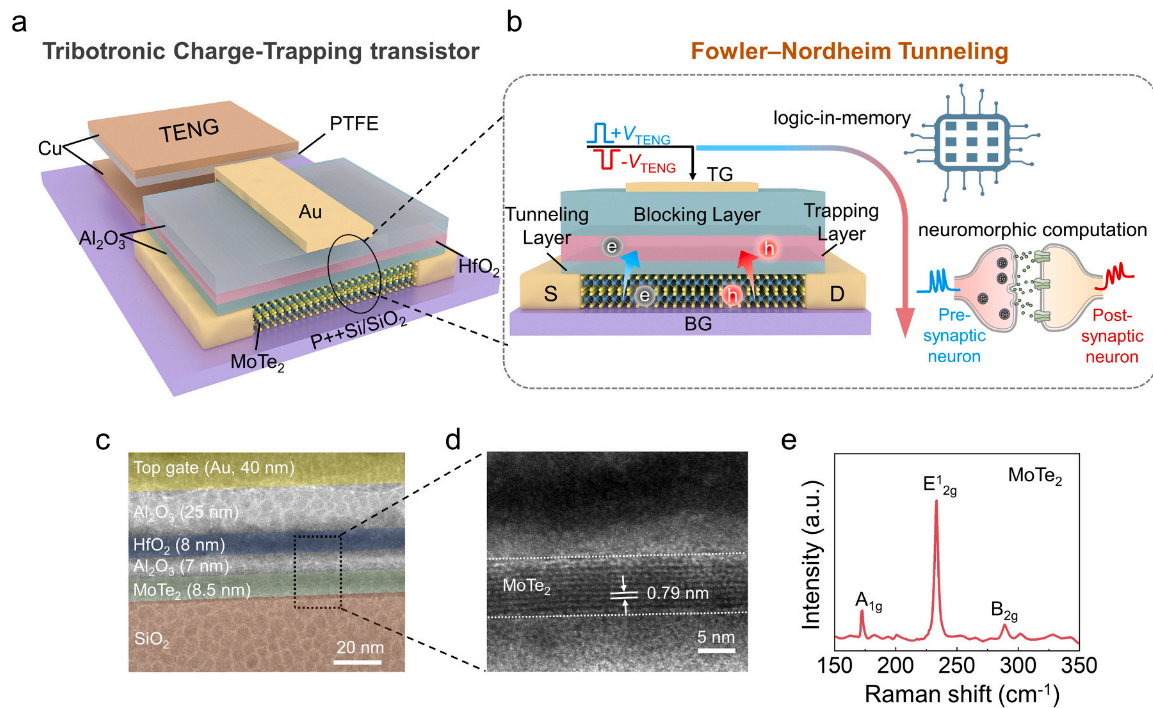

Fig. 1. Design of the neuromorphic triboelectric charge-trapping transistor. a) Schematic image of triboelectric charge-trapping transistor with $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack. b) Schematic diagram of the working principle of programming the charge-trapping $MoTe_2$ transistor using a V_{TENG} pulse. The grey and red circles are electrons and holes, respectively. The V_{TENG} generated by the TENG displacement is applied to the top gate. c) Cross-sectional TEM image of the triboelectric charge-trapping transistor. d) The TEM images of $MoTe_2$ layer are magnified in detail. e) Raman spectrum of the $MoTe_2$ with the characteristic peaks at $\sim$172 cm^{-1}($A_{1\,g}$), 233 cm^{-1}($E^1_{2\,g}$), and 288 cm^{-1}($B_{2\,g}$), confirming multilayer character of the utilized $MoTe_2$ [27,52,53].

charge-trapping process for mechano-driven logic-in-memory. Detailed device fabrication process is elaborated in Figure S2 and experimental section.

The control-gate design of $Al_2O_3/HfO_2/Al_2O_3$ (AHA) dielectric stack is highly effective in triboelectric charge-trapping process, where the HfO_2 layer (8 nm) serves as the charge-trapping layer and works synergistically with the 7 nm Al_2O_3 tunnelling layer for mechanical displacement assisted programming/erasing. Thereinto, the HfO_2 layer hosts numerous trap sites for capturing the mobile charges.[54] The difference in band alignment between HfO_2 and Al_2O_3 also results in the formation of a deep quantum well in the HfO_2 layer, with Al_2O_3 serving as a barrier to prevent the escape of captured charges to other layers. [55,56] Fig. 1b clearly illustrates the working mechanism of the triboelectric charge-trapping transistor for mechanical programming/erasing operations by controlling the magnitude and polarity of the coupled tribopotential V_{TENG} pulses, which involves triboelectric-assisted Fowler-Nordheim tunneling (F-N tunneling) and charge trapping process. [56,57] V_{TENG} mediated with triboelectric charges is coupled to the $MoTe_2$ channel and assist the charge carrier injection/storage process in the AHA dielectric stack, synergistically influencing the transport characteristics of the semiconductor channel.[58] The proposed triboelectric charge-trapping transistor can actively respond to mechanical instructions, record and process external information, and establish a direct interaction between electronic devices and ambient environment.

Prior to characterizing the electrical properties of triboelectric charge-trapping transistor, the influence of ALD deposition and detailed electrical performance of the charging-trapping $MoTe_2$ device are first examined in Figure S3 and S4. After the ALD deposition process for the AHA gate dielectrics, a significant improvement in device performance is observed in Figure S3, which is likely due to the effect of vacuum annealing and more effective screening of Coulomb scattering at the stacked dielectric-semiconductor interface.[59] The charging-trapping $MoTe_2$ device exhibits superior electrical output characteristics and typical memory properties (Figure S4). It is worth noting that after the deposition of the stacked gate, the bipolar $MoTe_2$ transistor shows the dominance of n-type behavior in the transfer curves, which may be related to the difference of the tunneling barrier height during the capture process of electrons and holes (Figure S5).[57]

The triboelectric charge-trapping transistor utilizes the tribopotential generated from the TENG unit to drive the device and modulate the transport characteristics of $MoTe_2$ semiconductor channel. To ensure reliable operation of the triboelectric charge-trapping transistor, it is essential to accurately understand the stability of V_{TENG} produced by the TENG unit (Figure S6) and corresponding gating mechanism (Figure S7). Under the precise control by a linear motor, the contact-separation distance in TENG unit is continuously varied at a constant speed, which can generate a continuous output voltage to serve as the scanning gate (i.e., V_{TENG}) for the transistor. Fig. 2a demonstrates the real-time transfer characteristic curve (drain current *vs.* TENG displacement, I_D-D_{TG}) of the triboelectric charge-trapping $MoTe_2$ transistor. Similar to the electrical transfer curve, the I_D-D_{TG} curve exhibits a large hysteresis window with a current on/off ratio of up to five orders of magnitude, and the magnitudes of the on-state (1.2 μA) and off-state (0.6 pA) currents are similar to that of the electrical transfer curve (Figure S3b). This hysteresis phenomenon may be attributed to the interface trapping occurring between $MoTe_2$ channel and SiO_2 dielectrics, primarily due to charge capture caused by oxide traps and adsorptive trap sites (such as moisture and oxygen). Typical tribotronic output performances are shown in Figure S8, exhibiting distinct output currents corresponding to different D from −0.04 to +0.24 mm stepped by 0.04 mm. These results demonstrate that the tribopotential can successfully replace the gate voltage (V_G) to drive the transistor. For non-volatile memory, faster scanning speed can provide higher operation speed for faster writing/reading process. Therefore, we also study the influence of scanning speed on the memory window of the triboelectric charge-trapping $MoTe_2$ transistor. Fig. 2b shows the relevant I_D-D_{TG} curve under different scanning speeds of mechanical displacement D. The slight decrease in the memory window may be attributed to incomplete charge

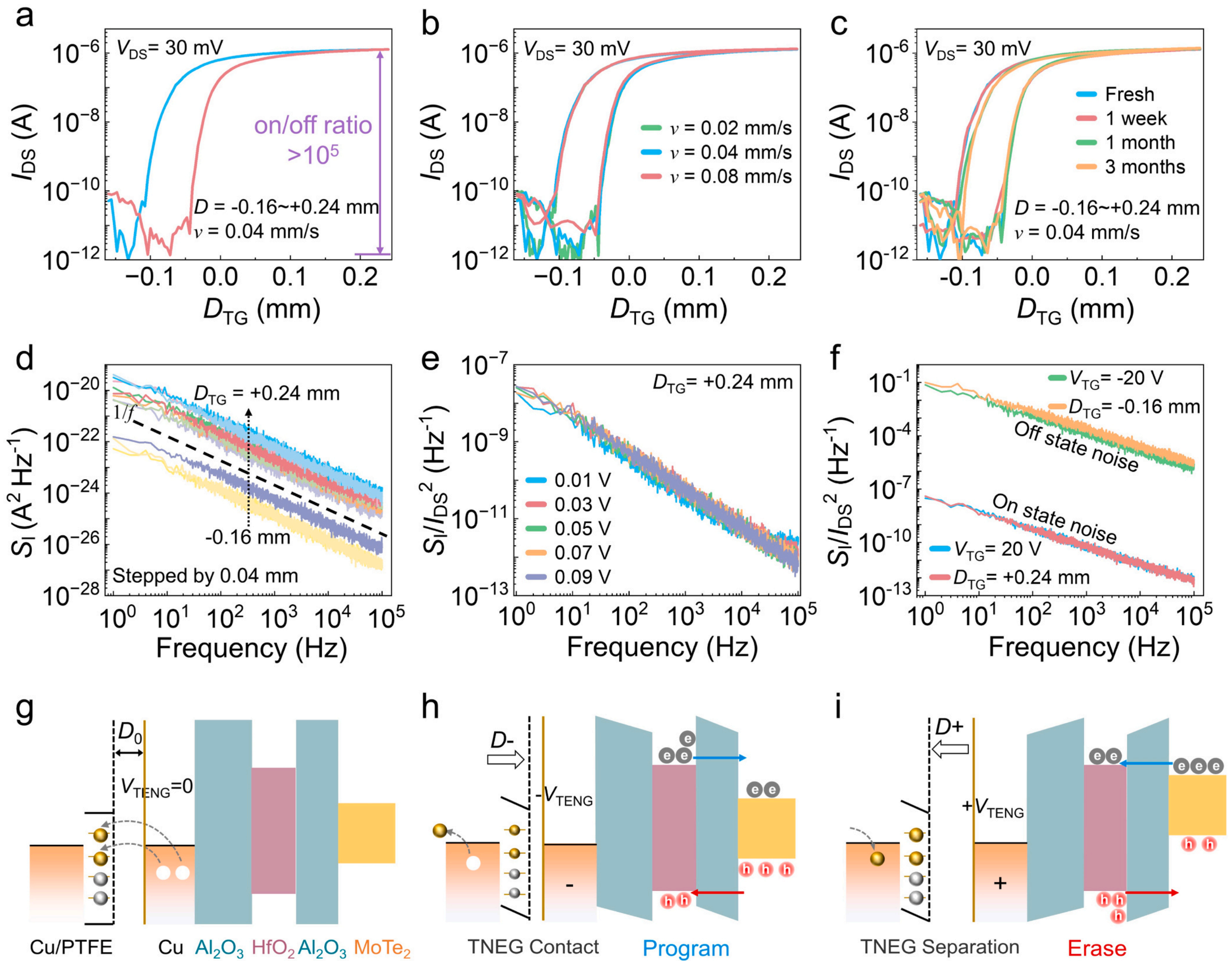

Fig. 2. Electrical characterization on the triboelectric charge-trapping transistor. a) Transfer curve of triboelectric charge-trapping transistor. b) Transfer curve of triboelectric charge-trapping transistor at different sweep rates. c) Transfer curve of triboelectric charge-trapping transistor over three months. d) The S_I of the triboelectric charge-trapping transistor under different TENG displacements (ranging from −0.16–0.24 mm stepped by 0.04 mm). e) The S_I/I_{DS}^2 of the triboelectric charge-trapping transistor at different V_{DS}. f) The S_I/I_{DS}^2 of the on and off states is controlled separately by voltage and triboelectric potential. Energy band diagram of the charge trapping mechanism of the device under g) zero V_{TENG}, h) positive V_{TENG}, and i) negative V_{TENG}, respectively.

trapping induced by the over-fast scanning speeds (Figure S9c). Similar phenomena have already been observed under conventional gate voltage scanning (Figure S9a). To further validate the excellent stability of the triboelectric charge-trapping transistor, real-time dynamic test is conducted by evaluating the I_D variation, which shows a positive response to the gradually decreased displacement from +0.24 to −0.08 mm (in 0.04 mm step) and stabilizes at a certain value (the I_D drops in a stepwise manner from 1.2 μA to 1 pA, on/off ratio = 10^5, Figure S10). The real-time current variation under 50 consecutive cycles of contact-separation operations shows no significant differences (Figure S11), indicating excellent durability of the device. Notably, thanks to the antioxidative encapsulation of $MoTe_2$ active layer via 40 nm-thick AHA dielectric stack deposited by ALD, the electrical performances of the triboelectric charge-trapping transistor show almost no deviation even after recording for over three months (including the storage window, on-/off-state currents, and switching ratio, Fig. 2c).

As is known, channel current noises generally exist in transistor device and exhibit $1/f$ noise characteristics at low frequency. To investigate the current fluctuation mechanism of the AHA dielectric stack gated by tribopotential and exclude any probable current noise induced by the mechano-driven process, we conduct the low-frequency noise and impedance spectroscopy on the triboelectric charge-trapping transistor under different V_G and V_{TENG}. Under either V_G or V_{TENG} gating effect, the low-frequency noise (S_I) of the charge-trapping device exhibits an increasing tendency with increasing V_{TG} and V_{TENG} in the frequency range of 2 Hz to 100 kHz at the fixed drain voltage (V_D) of 30 mV (Fig. 2d and Figure S12), displaying the characteristic $1/f$ noise dependency. Fig. 2e and Figure S12b depict that the normalized source-drain current noise spectral density (S_I/I_D^2) is independent of V_D, indicating that the noise signal is primarily influenced by the intrinsic current conduction characteristics of the $MoTe_2$ channel, rather than the contact barrier between the channel and source-drain electrodes (also implying the well-formed Ohmic contact during the ALD deposition process).[60] In addition, the S_I/I_D^2 states in the on and off states under both V_G and V_{TENG} modulations are also compared in Fig. 2f, exhibiting two highly overlapped profiles consistent with the ideal $1/f$ noise signals. All the above results indicate that the triboelectric charge-trapping transistor exhibits typical low-frequency noise behaviors following the $1/f$ noise pattern, which is similar with the traditional device modulated by V_G. It is critical that mechano-driven process does not introduce additional current disturbance and ensure the reliability of the triboelectric charge-trapping transistor for theoretical research and practical

applications.

By analyzing the band alignment of $MoTe_2$-AHA dielectric stack under V_{TENG} gating, we can approximately depict the energy band diagram of the triboelectric charge-trapping transistor under different working conditions as shown in Figs. 2g to 2i. The schemes illustrate the band diagram and charge transfer process of the device under three conditions of zero, negative, and positive tribopotential. At the initial state with the preset displacement D_0, there is no charge transfer to the top gate electrode under zero tribopotential (*i.e.*, $V_{TENG} = 0$ V), and the device is in a flat band state (Fig. 2g). When the TENG is in the D_- state, the charge balance is disrupted, leading to the induced and unbounded electrons transfer from the fixed Cu electrode to the top gate, equivalent to applying a negative gate voltage (-V_{TENG}, consistent with the contact process in Figure S7). As the relative distance between the Cu electrode and PTFE/Cu layer decreases, -V_{TENG} will also decrease. Under a sufficiently negative V_{TENG}, the energy band of the Al_2O_3 dielectric layer will bend into a triangular barrier with a reduced width. Thus, by controlling the magnitude of V_{TENG}, we can modulate the thickness of the dielectric barrier and control whether electrons or holes can tunnel through the Al_2O_3 barrier and inject into the HfO_2 trapping layer. Under -V_{TENG} gating, the accumulated holes in $MoTe_2$ channel tunnel through the Al_2O_3 barrier and get injected into the HfO_2 trapping layer, where they can be captured and retained (red arrow in Fig. 2h). Simultaneously, the residual electrons in the HfO_2 layer can drift back into the $MoTe_2$ channel through the field emission effect (blue arrow in Fig. 2h). In this circumstance, both of the charge carrier behaviors lead to the tribotronic threshold value (D_{TH}) shift in the D_- direction (blue curve in Fig. 2a). In the third situation of Fig. 2i, when the Cu electrode separates from the PTFE/Cu layer (D_+ state), some of the induced electrons flow to the ground and weaken the confinement between the electrons in PTFE and the remaining positive charges in the fixed Cu film. As a result, some positive charges accumulate at the top gate and Al_2O_3 interface, creating an equivalent positive gate voltage ($+V_{TENG} > 0$ V, consistent with the separation process in Figure S7). In this case, the trapped holes will be repelled back into the channel by the tribopotential, while the electrons tunnel through the Al_2O_3 barrier through the F-N tunneling and get injected into the HfO_2 trapping layer (Fig. 2i). Thus, under $+V_{TENG}$, the tribotronic threshold D_{TH} will shift to the D_+ direction (red curve in Fig. 2a). The detailed analysis on energy band diagram demonstrates the induced tribopotential can effectively modulate the energy band and barrier width of the AHA dielectric stack, and enable efficient charge capture and release, which lays the foundation for the mechano-driven logic-in-memory and artificial synaptic features.

Based on the above discussed reliable charge transport/trapping mechanism assisted with mechanical displacement, we further explore the potential application of the triboelectric charge-trapping transistor as a mechano-driven multibit memory device. Fig. 3a shows a single-cycle dynamic operation of the memory, including programming, reading, and erasing processes. The programming operation is achieved by applying a D_- pulse to the memory device ($D_{PRO} = -0.16$ mm, width $= 0.5$ s, corresponding V_{TENG} pulse = ~-20 V). Under the influence of -V_{TENG}, the holes in $MoTe_2$ channel tunnel through the Al_2O_3 barrier and accumulate in the HfO_2 trapping layer. Due to the high energy barrier of the AHA stack gate, the holes remain stably stored in the HfO_2 trapping layer even after removing the pulse. The accumulation of holes in the HfO_2 trapping layer generates a local positive electric field, leading to a high concentration of electrons in the $MoTe_2$ channel with a highly conductive and readable state (on-state). As shown in Fig. 3a, I_D shows a sharp increment in current after the mechanical programming, stabilizes at ~550 nA, and remains stable even after 200 seconds, indicating the typical non-volatile characteristics of the triboelectric charge-trapping transistor. The device can also be reset to a low-conductive state by applying an erasing D_+ pulse ($D_{PRO} = 0.24$ mm, width $= 0.5$ s, resulting in $+V_{TENG} = \sim 20$ V). During this process, the holes trapped in the HfO_2 trapping layer are repelled back to the $MoTe_2$ channel (off-state). The recorded transient current after erasing is 61 pA and shows a subsequent

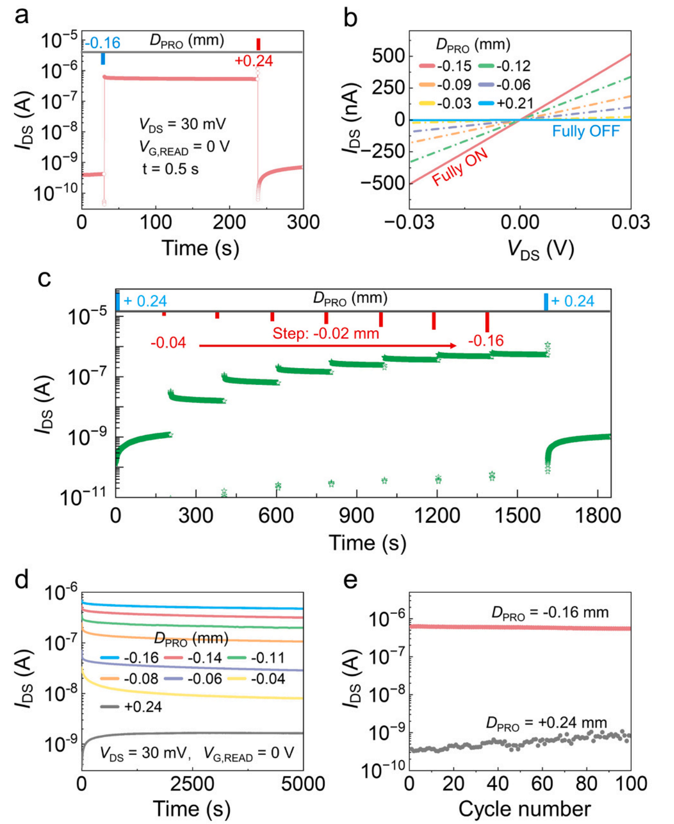

Fig. 3. Triboelectric charge-trapping transistor for non-volatile memory. a) Demonstration of single-cycle program-read-erase operations for the memory. b) Output characteristics (I_D-V_D) of the memory after programming with different programming displacements (D_{PRO}), with $V_D = 30$ mV and $V_{G,\ READ} = 0$ V. c) Dynamic memory properties responding to the different D_{PRO} sequence of Program-Read-Erase-Read. d) Retention performance of memory, the current is read after programming with $V_D = 30$ mV and $D_{TG} = 0$ mm. e) The endurance of the memory device for 100 cycles program (-0.16 mm, 0.5 s) and erase (+0.24 mm, 0.5 s) operations.

increment to ~0.7 nA after 60 seconds, which may be attributed to some repelled holes re-entering the channel. Fig. 3b shows the output curves (I_D-V_D) of the triboelectric charge-trapping transistor programmed by different D_{PRO} at $V_D = 30$ mV. The linear relationship between I_D and V_D further confirms the good Ohmic contact, which can effectively reduce the energy loss and heat generation and enhance the reliability of the transistor and memory performance.

By varying the amplitude of D_{PRO} pulses (ranging from -0.04 to -0.16 mm, width $= 0.5$ seconds), a dynamic multi-level memory behavior can be achieved in the triboelectric charge-trapping transistor. As shown in Fig. 3c, I_D varies from 1.7×10^{-9} to 5.3×10^{-7} A, yielding eight distinguishable and stable current levels (equivalent to 3 bits). Initially, the device is reset to a low-conductive state with a programming pulse of +0.24 mm. As consecutive D_{PRO} pulses are applied with increasing amplitudes, the charge-trapping state can be readily controlled with I_D programmed into eight clear readout values. In memory device, the programming speed is a crucial factor to evaluating the electrical performances. The fabricated charge-trapping transistors in this work can conduct effective programming process even under the electrical writing pulse with 2-millisecond width, which also exhibits commendable repeatability (Figure S13). In practical applications, excellent charge retention and durability during cycling programming/erasing are another crucial factor for memory devices. Fig. 3d shows the reliable retention performance of the memory under multiple programming/erasing states, in which seven distinguishable conductive states can be maintained steadily even after 5×10^3 seconds (on/off ratio

$> 3\times10^2$). Moreover, further monitoring on the programming/erasing states for up to 10^4 seconds reveal almost no significant degradation or deterioration in the device and promises with an industry-standard 10-year data retention performance (Figure S14). To evaluate the durability of the memory, we perform cyclic programming ($D_{PRO} = +0.24$ mm, width $= 0.5$ s) and erasing ($D_{PRO} = -0.16$ mm, width $= 0.5$ s) process to implement the switching between the low and high conductive states. As shown in Fig. 3e, after 100 cycles, there is almost no change in the programming/erasing current ratio, demonstrating the device's excellent fatigue resistance. In addition, we have also investigated the mechano-driven memory properties for over three months, which reveal no significant fluctuations in writing, reading, erasing, and retention characteristics (Figure S15). The outstanding retention and reliability further confirm the highly efficient and stable TENG gating and the excellent charge trapping capability of the tribotronic device.

As the TENG unit can readily set the state of the charge-trapping memory by using a programming displacement D_{PRO}, a mechano-driven programmable inverter with non-volatile characteristics can be constructed by connecting a 50 MΩ resistor in series with the triboelectric charge-trapping transistor (equivalent circuit diagram in Fig. 4a). In this circuit, the source of the triboelectric charge-trapping transistor is connected to the PTFE/Cu layer and grounded, while the drain is connected to the 50 MΩ resistor as the output terminal (V_{OUT}). Additionally, the top gate is connected to the fixed Cu layer serving as both the programming port for setting the transistor's conduction state and as the input terminal (D_{IN}) for driving the inverter during logic operations. Based on the non-volatile programmable characteristics of the triboelectric charge-trapping transistor, we can precisely control the charge capture/release properties in the AHA structure via mechanical displacement, readily realize the modulation on the transistor's switch threshold (D_{TH} or V_{TH}). As shown in Figs. 4b and 4c, according to the screening efficiency of the captured charges in the AHA structure, the discrete memory states in the triboelectric charge-trapping transistor can be roughly divided into three types (equivalent circuit diagrams in Figure S16). When a larger D_{-} pulse is applied to program the device ($D_{PRO} = -0.16$ mm, width $= 1$ s), the holes tunnel into the HfO_2 layer with the left electrons strongly doping the $MoTe_2$ channel. In this state, the equivalent circuit is similar to a short circuit status, labelled as

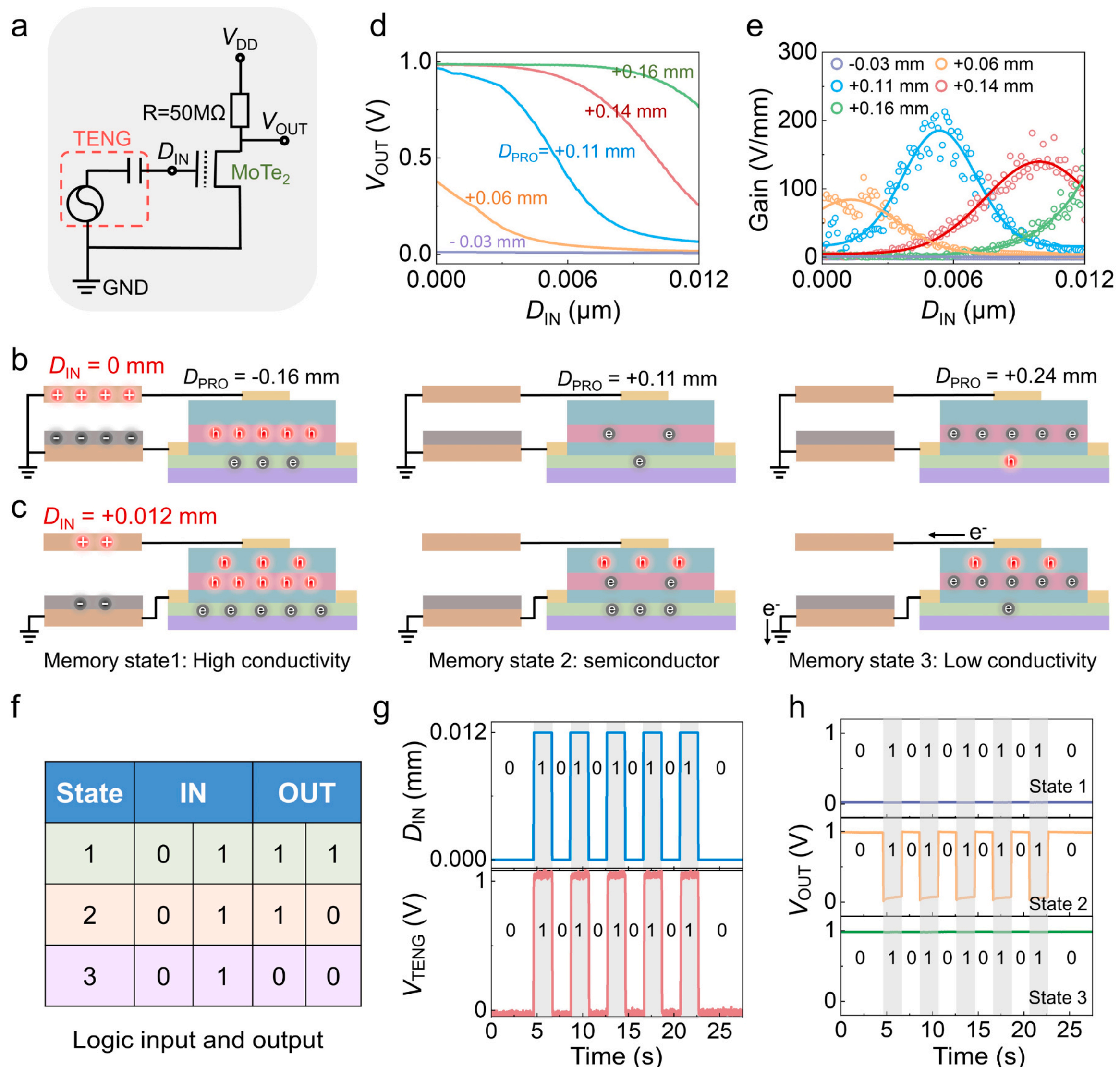

Fig. 4. Nonvolatile programmable inverter based on triboelectric charge-trapping transistor. a) Equivalent circuit diagram of the TENG-driven nonvolatile programmable inverter. b) and c) The working principle and operation process of the inverter at $D_{IN} = 0$ mm and $D_{IN} = +0.012$ mm with three memory states. d) The voltage transfer characteristics of inverter at $V_{DD} = 1$ V for different programming conditions as D_{IN} increases from 0 to 0.012 mm. e) Corresponding voltage gains under different programming conditions. f) Truth table of the inverter under three states. g) The upper part shows the dynamic displacement D_{IN} and corresponding V_{TENG} input. h) The logic computation in three different programming states.

memory state 1. In contrast, when a positive D_+ pulse is applied to the device (D_{PRO} = +0.24 mm, width = 1 s), the n-type dominant $MoTe_2$ channel is depleted and exhibits low conductivity characteristics. The equivalent circuit is similar to an open-circuit circumstance, and we label this state as memory state 3. In state 2, when a smaller programming displacement pulse is applied (D_{PRO} = +0.11 mm, width = 1 s), the captured charges in the AHA structure cannot fully screen the input signal at the gate. In this state, the $MoTe_2$ channel exhibits normal semiconductor characteristics, which allow the device to operate as a regulating transistor for inverter applications without the influence of captured charges.

For the mechano-driven programmable inverter, the input displacement D_{IN} range is set from 0 to 0.012 mm, corresponding to tribopotential ranging from 0 to 1.1 V (representing the input logic from “0” to “1”). To prevent the device from being reset by excessive voltage, we reasonably constrain the input tribopotential within the range of 0–1.1 V and use 1 V as the supply voltage (V_{DD}). Fig. 4d illustrates the output voltage transfer curve of the inverter under different mechano-driven programming states, with D_{PRO} ranging from −0.03 to +0.16 mm. The transfer curve shows that the logic level of the inverter varies at different programming states. Fig. 4e depicts the corresponding gain values defined by -dV_{OUT}/dD_{IN} extracted from the tribotronic voltage transfer curves. The maximum voltage gain of 212 V/mm is obtained at a programming displacement of +0.11 mm. The data points represent the actual extracted values from the transfer curves, while the solid line represents the results obtained through formula fitting. The basic electrical characterizations on the inverter based on the charge-trapping $MoTe_2$ transistor are shown in Figure S17, which exhibit similar transfer behaviors to that under TENG driving. Based on the aforementioned three mechano-programming states by tribopotential, we further investigate the dynamic switching behavior of the inverter as illustrated in Fig. 4f, which shows that the V_{OUT} and corresponding logic states of the programmable inverter are associated with both the D_{IN} and the transistor state. Fig. 4g displays the contact-separation motion

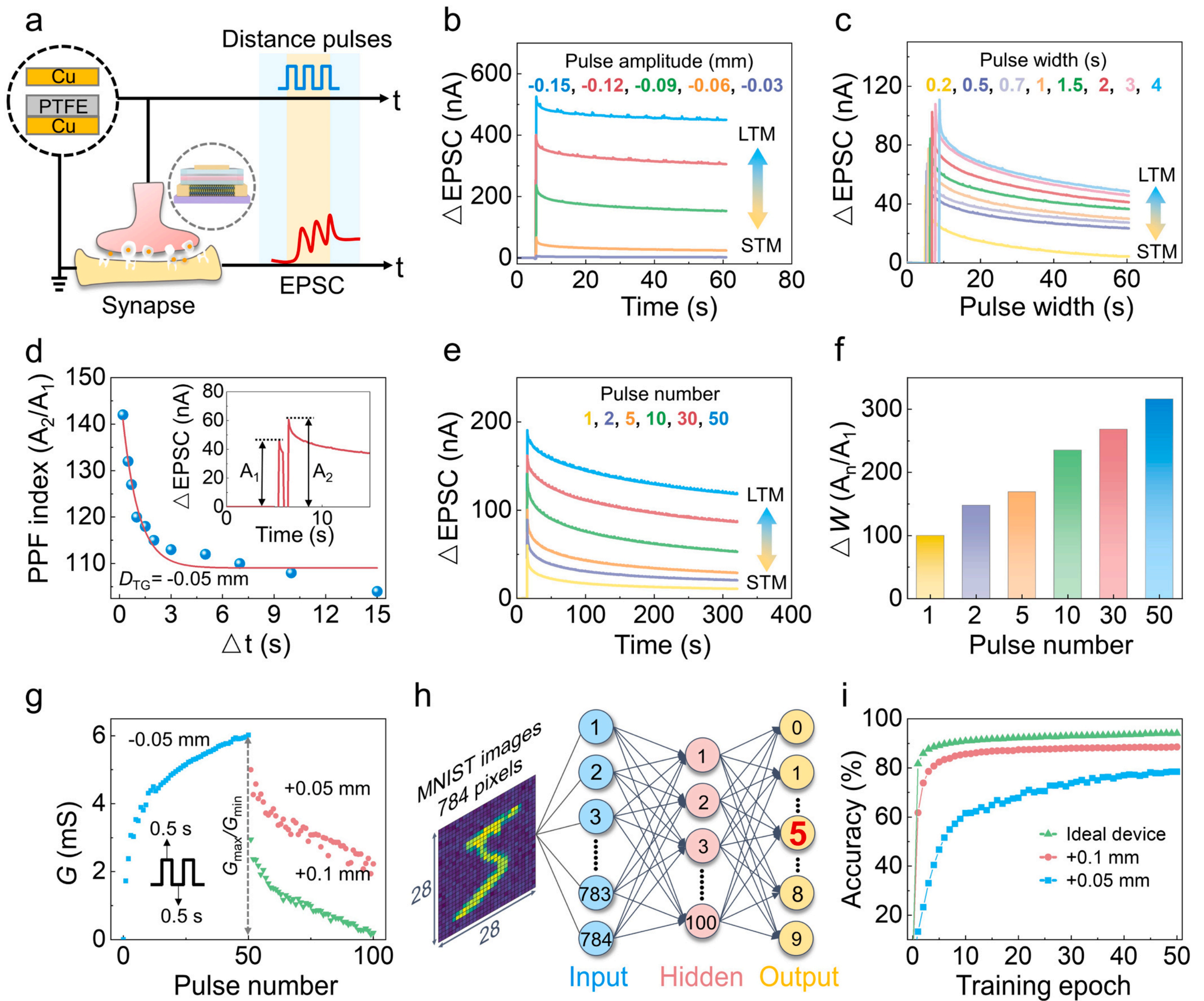

Fig. 5. Neuromorphic memory based on triboelectric charge-trapping transistor. a) PSC triggered by mechanical displacement pulse. b) EPSCs triggered by applying several displacement pulses with different amplitudes. c) EPSCs triggered by applying several different durations of displacement pulse (D = −0.05 mm, Δt = 0.5 s). d) Extracted PPF index (A_2/A_1) vs. pulse time interval Δt. The inset shows a typical response of EPSC triggered by a pair of D pulse. e) EPSC is triggered by applying different numbers of displacement pulse. f) The synaptic weight (defined as the ratio of A_n/A_1) with different pulse numbers. g) The potentiation and depression of the conductance (G) extracted from triboelectric charge-trapping transistor under 100 successive input pulses. The reading voltage is V_{DS}= 30 mV. (Potentiation: D = −0.05 mm, duration of 0.5 s, Δt = 0.5 s; Depression: D = +0.05 mm or +0.1 mm, duration of 0.5 s, Δt = 0.5 s). h) Illustration of the three-layer perceptron ANN used for recognition tasks. i) Comparisons of the recognition accuracy with training epochs for handwritten digit images.

trajectory of TENG under linear motor control (square wave with a width of 2 s) and the corresponding V_{TENG} as the input signal. When the device is programmed in state 1, the triboelectric charge-trapping transistor is in a high-conductance state. In this state, the input signal does not affect the output voltage, which remains at a low level (logic output state "0", top graph in Fig. 4h). When the device is in state 2, it exhibits the transient characteristics of an inverter, demonstrating a stable logic inversion (middle graph in Fig. 4h). In state 3, the triboelectric charge-trapping transistor is configured in a high-resistance state, which leads to the output signal remains at a high level during the logic operation (denoted as logic state "1", bottom graph in Fig. 4h). Compared with the common logic gate technologies, the mechano-driven programmable inverter based on the triboelectric charge-trapping transistor provides additional degrees of freedom for applications in digital and analog circuits and achieves low-power-consuming logic conversion by external mechanical motion, which offers an efficient approach to reducing the circuit complexity and power consumption in the future.

Inspired by the biological tactile system, the mechano-driven logic-in-memory function of the triboelectric charge-trapping transistor can be further extended for emulating the biological sensory and memory neuron. As shown in Fig. 5a, biological synapses transmit signals through the neurotransmitters in the synaptic cleft. These neurotransmitters bind to receptors on the post-synaptic neuron, trigger the opening/closing of ion channels, and alter the neuron's membrane potential to achieve signal transmission. In the triboelectric charge-trapping transistor, the TENG unit can mimic the mechanical sensor to transmit pre-synaptic signals, while the charge-trapping $MoTe_2$ transistor serves as the synaptic device by capturing and releasing charges to emulate the signal transmission behavior between different neurons. The top-gate/drain electrode of the charge-trapping transistor is defined as the pre-/post-synaptic terminal; the source-drain current represents the post-synaptic current (PSC); $MoTe_2$ channel conductance represents the synaptic weight (w). Tribopotential induced by mechanical displacement pulse D with spatiotemporal information can be coupled to the synaptic transistor to control the charge-trapping behaviors in the AHA stack dielectrics, thereby modulating the channel's conductive state to achieve the synaptic plasticity. We first investigate the influence of amplitude (spatial information) and width (temporal information) of the mechanical displacement pulse D on the triggered EPSC behavior. As shown in Figs. 5b and 5c, when two different sets of mechanical displacement pulses are applied, all the $\triangle$EPSC curves undergo a rapid increase with slow decay. Fig. 5b displays the $\triangle$EPSC significantly increases from 5.6 to 525.2 nA as the pulse amplitude increases from 0.03 to 0.15 mm at a fixed pulse width of 0.5 s, which indicates enhanced excitatory synaptic behavior. This result is attributed to that larger amplitude D pulses generate higher tribopotential, induce more holes to accumulate in the AHA stack, and heavily dope the $MoTe_2$ channel to produce a higher $\triangle$EPSC. A similar trend is observed by increasing the duration of the mechanical displacement pulse (Fig. 5c). When the duration increases from 0.2 to 4 s at a fixed D pulse of -0.05 mm, the peak value of $\triangle$EPSC gradually increases. Longer durations of D pulses allow more holes to have sufficient time to be trapped into the AHA stack, leading to an increased electron concentration in the channel and a resultant larger EPSC. To further understand the synaptic plasticity of the device, we investigate the PPF behavior triggered by D, which is considered a typical STM feature of synapses. By simply applying a pair of D pulses to the triboelectric charge-trapping transistor, Fig. 5d shows the PPF index (PPF index $= (A_2/A_1)\times 100\%$, A_1 and A_2 represent the peak values of the first and second EPSC) decreases from 142% to 104% with the increasing time interval (Δt) of D pulse (-0.05 mm), which fits well with a double exponential decay function (red line). This phenomenon is due to the partially trapped holes in the AHA gate stack have enough time to diffuse into the channel and reach equilibrium, making A_2 approach A_1 gradually.

In neuroscience, memory can be classified into two types based on the duration of retention: STM and LTM.[7,61] Similarly, the triboelectric charge-trapping transistor can adjust the synaptic connection strength by modulating the width, amplitude, and number of D pulses, enabling the transition from STM to LTM (Figure S18a). As shown in Fig. 5e, when the number of D pulses increases from 1 to 50, the memory level of the artificial synapse is significantly enhanced, indicating a transition from STM to LTM. This transition is also influenced by the width and amplitude of the D pulses as observed in Figs. 5b and 5c. Corresponding synaptic weight ($\Delta W = A_n/A_1$, A_n represents the $\triangle$EPSC triggered by the nth D pulse), which represents the change in synaptic connection strength (or weight) triggered by the mechanical displacement pulses, is extracted as shown in Fig. 5f. The ΔW gradually increases from 100% to 316%, indicating a successful mimicking on the learning and memory patterns of the brain. Based on this characteristic, we have tried to emulate the "learning-memory-forgetting" behaviors with the mechano-driven charge-trapping transistor by applying two consecutive displacement pulse sequences ($D = -0.05$ mm, width of 0.5 second, separated by a 0.5-second interval). Figure S18b demonstrates that during the "relearning" process, after a period of stimulation (5 times, around 5 seconds), the channel current recovers to a higher level, achieving the same cognitive level with reduced learning process.

Energy consumption is a critical factor when constructing neuromorphic computing systems by using artificial synapses. For the triboelectric charge-trapping transistor, the gate control voltage is entirely replaced by the tribopotential, and the source-drain bias can be reduced to as low as 0.5 mV. Utilizing the formula $E = V_D \times I_{peak} \times t$ (where I_{peak} is the peak current, V_D is the source-drain voltage, and t is the pulse width), the energy consumption of single synaptic event can be reduced to 147 fJ (1.47 nA, 0.5 mV, 0.2 s), which shows a comparable level with that of the biological neurons (1–100 fJ, illustrated in Figure S19a).[44] Moreover, we have also provided a comparison of synaptic energy consumption in Table S2, which indicates the triboelectric charge-trapping transistor is comparable to or even better than the power consumption of most charge-trapping synaptic transistors. In fact, the mechanical displacement modulation in the charge-trapping process contributes to the elimination of energy dissipation associated with V_G charging process, thereby reducing the overall energy consumption. This result indicates the prepared synaptic devices can achieve the energy efficiency levels comparable to biological neural systems, showcasing significant potential for further neuromorphic computing and in-sensor computing in low-energy conditions. Furthermore, we evaluate the potentiation and depression of the synaptic weight (channel conductance) updated by mechanical displacement pulses. As shown in Fig. 5g, a series of 50 consecutive D_- pulses (-0.05 mm, width of 0.5 seconds, and time interval of 0.5 seconds) are applied, followed by another set of 50 consecutive D_+ pulses (+0.05 mm, width of 0.5 seconds, and time interval of 0.5 seconds) to obtain the update trajectory of the synaptic weight (channel conductance). It's worth noting that during the long-term depression process, applying 50 consecutive D_+ pulses does not completely erase the trapped holes stored in the AHA stack structure. This is attributed to the relatively high tunneling barrier of the AHA stack, and the tribopotential generated by the +0.05 mm is not sufficient to erase the trapped holes. However, by increasing D_+ (+0.1 mm), the initial conductivity of the channel can be restored (Fig. 5g). Changing the displacement pulse amplitude can effectively help to achieve different erasing levels.

The successful dynamic updating on the synaptic weight through D pulses demonstrates the potential of this device in the field of neuromorphic computing. Based on this, we have constructed an ANN for supervised learning of handwritten digits using the triboelectric charge-trapping transistors and a three-layer perceptron network model. As depicted in Fig. 5h, the ANN comprising 784 input neurons, 100 hidden layer neurons, and 10 output neurons is in full connection among the three layers through synaptic weights (conductance). The binarized images of handwritten digits (28 × 28 pixels) are sourced from the MNIST dataset.[62] During the supervised learning process, ANN

utilizes the sigmoid activation function for vector transformation and employs the backpropagation learning algorithm to update the synaptic weights. Based on this approach, the neural network is initially trained using 60,000 training images, and then classified with 10,000 test images (additional ANN simulation details in the **Supplementary Note 1**). Fig. 5i displays the relationship between recognition accuracy and the number of training epochs at different depression displacements (D_+). After 50 training epochs, with an increase in D_+ (resulting in a higher G_{max}/G_{min} ratio, as shown in Figure S20), the recognition accuracy is improved from 78.43% to 88.59%. This result indicates a positive impact of higher conductance ratios on the recognition accuracy of MNIST images. The nonlinearity of the potentiation and depression curves is another crucial factor affecting recognition accuracy.[63,64] The training performance of the fabricated devices falls slightly below the ideal scenario, but it can be improved by optimizing the stack gate thickness and employing different displacement pulse schemes to increase G_{max}/G_{min} and reduce nonlinearity, consequently enhancing the recognition accuracy. In addition, a confusion matrix for handwritten digit prediction with a depression displacement of +0.1 mm is also provided, as shown in Figure S21. It presents a comprehensive view on the network's classification performance, enabling a clear assessment of prediction accuracy, error proportions, and categories. The results indicate that digit 1 exhibits the best classification performance, while digit 8 is the most prone to errors (82.75%). These results demonstrate the outstanding mechanical-driven pattern recognition performance with the triboelectric charge-trapping transistors.

3. Conclusion

In summary, we have successfully demonstrated a mechano-driven logic-in-memory device for neuromorphic computation. This is achieved through the proposed triboelectric charge-trapping transistor. Upon the mechanical displacement of the integrated TENG unit, the triboelectric charges mediated tribopotential can effectively modulate the $MoTe_2$ transistor using the AHA stack dielectrics, which allow the charge carriers to tunnel and store in the HfO_2 charge-trapping layer. The triboelectric charge-trapping transistor exhibits excellent mechanical behavior derived electrical properties and memory characteristics. Additionally, a mechano-programmable resistor-loaded inverter has been developed for implementing logic switching via TENG displacement. We have also successfully emulated a femtojoule (~147 fJ) mechanoplastic artificial synapse, demonstrating essential synaptic functions and achieving an 88.59% accuracy in a three-layer perceptron ANN learning on the MNIST dataset. The proposed triboelectric charge-trapping transistor holds significant promise for advanced mechanical-assisted interactive interfaces, low-energy logic-in-memory systems, and mechano-neuromorphic computation.

4. Experiments

4.1. Device fabrication

The few-nanometer-thick 2 H-$MoTe_2$ flakes (99.995%, HQ Graphene) after mechanical exfoliation were transferred onto n-doped silicon wafers (with a SiO_2 thickness of 300 nm). Then, source and drain electrodes were defined using standard electron beam lithography and etching techniques. The channel (length of 2 μm) was defined by depositing a 7 nm/20 nm Cr/Au electrode on the transferred channel material using thermal evaporation. An $Al_2O_3/HfO_2/Al_2O_3$ stack gate with layer thicknesses of 7/8/25 nm was deposited using ALD, where the HfO_2 layer (8 nm, grown at 300℃) acted as the charge-trapping layer, working in synergy with the Al_2O_3 layer (7 nm, grown at 120℃) to achieve charge trapping and erasing functions. Finally, a 40 nm-thick top gate electrode (gold) was deposited using the same process for source/drain electrodes. The triboelectric nanogenerator consisting of a Cu/PTFE/Cu structure was integrated with the $MoTe_2$ charge-trap transistor via the top gate electrode to form triboelectric charge-trapping transistor, as shown in Figure S2.

4.2. Characterizations

The Raman characteristics of $MoTe_2$ were measured using a HORIBA/LabRAM HR Evolution spectroscope with an excitation laser wavelength of 532 nm and a power of 25%. The morphology and thickness of the $MoTe_2$ thin film were characterized using AFM (Agilent Technologies 5500 AFM/SPM System). The device cross-section was obtained using focused ion beam (FIB) milling, and TEM analysis was performed to analyze the stacked gate structure and channel material. During the device performance testing, the TENG units were driven by a programmable linear motor controlled by a computer, which provided precise displacement control to generate the desired V_{TENG}. The Keithley 6514 system was utilized to record the output voltage of the TENG unit. All electrical and tribotronic performance measurements of the device were conducted at room temperature in an air ambient using the Agilent B1500A semiconductor device analyzer.

4.3. ANN simulation

A three-layer ANN for MNIST pattern recognition was adopted with a network size of 784×100×10. The MNIST dataset consisted of 60,000 training images and 10,000 test images, each with a size of 28×28 pixels. In the ANN simulation, the backpropagation algorithm was utilized for weight updates. The hidden layer employed the sigmoid activation function for vector transformation, and the output layer used Softmax. Ideal devices referred to software virtual components that exhibited perfect synaptic characteristics, with entirely linear conductance weight updates (curvature equals zero).

CRediT authorship contribution statement

Zhong Lin Wang: Investigation. **Qijun Sun:** Writing – review & editing, Writing – original draft, Validation, Supervision, Project administration, Funding acquisition, Conceptualization. **Yichen Wei:** Writing – original draft, Methodology, Investigation, Conceptualization. **Jinran Yu:** Investigation. **Yonghai Li:** Investigation. **Yifei Wang:** Investigation. **Ziwei Huo:** Investigation. **Liuqi Cheng:** Investigation. **Dewu Yue:** Writing – review & editing, Validation, Supervision, Investigation, Conceptualization. **Keteng Zhang:** Investigation. **Jie Gong:** Investigation. **Jie Wang:** Investigation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.nanoen.2024.109622.

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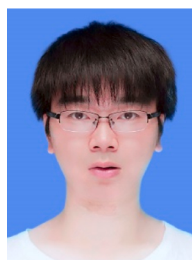

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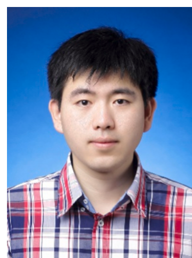

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