



Full paper



Enhanced performances of AlGa_N/Ga_N HEMTs with dielectric engineering of HfZrO_x

Xiao Cui^{a,b}, Weijun Cheng^c, Qilin Hua^{a,b,**}, Renrong Liang^c, Weiguo Hu^{a,b,d,*},
Zhong Lin Wang^{a,b,d,e,***}

^a CAS Center for Excellence in Nanoscience, Beijing Key Laboratory of Micro-nano Energy and Sensor, Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing, 100083, China

^b School of Nanoscience and Technology, University of Chinese Academy of Sciences, Beijing, 100049, PR China

^c Institute of Microelectronics, Tsinghua University, Beijing, 100084, PR China

^d Center on Nanoenergy Research, School of Physical Science and Technology, Guangxi University, Nanning, 530004, PR China

^e School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA, 30332-0245, USA

ARTICLE INFO

Keywords:

AlGa_N/Ga_N
Dielectric
HEMT
High-κ
HfZrO_x

ABSTRACT

III-nitrides based high electron-mobility transistors (HEMTs) are well-known excellent candidates for high-power, radio-frequency (rf) and high-temperature applications. However, HEMTs have to face the essential issues of high gate leakage current and drain current collapse (gate-lag), which inevitably limits the device performances and reliability. Here, we fabricate an optimized AlGa_N/Ga_N metal-oxide-semiconductor high electron mobility transistor (MOS-HEMT), by using HfZrO_x (HZO) as a gate dielectric, that can improve the interfacial and transport properties. Compared to the conventional high permittivity (high-κ) gate dielectric HfO₂ which has attracted wide attention in recent years, the concentrations of interface traps and the inside fixed oxide defects are obviously reduced by using high quality HZO layer. Through the dielectric engineering of HZO, the MOS-HEMT with HZO dielectric shows an enhanced DC output performance with an increase of 54% at the optimal working condition, which is indeed much higher than that of the HfO₂ MOS-HEMT (40%). And the HZO MOS-HEMT exhibits a higher I_{on}/I_{off} ratio of 10^6 , an excellent subthreshold swing (SS) of 85 mV/decade, and a higher voltage swing (GVS). The gate leakage is reduced by nearly 8 orders of magnitude compared to the conventional unpassivated HEMTs (conv. HEMT) at the gate voltage of -5 V. These results are mainly caused by the replacement of the low-height Schottky barrier (SB) and the reduction of interface traps density. In order to further investigate the interfacial and electric properties of HZO MOS-HEMT, the dynamic gate/drain voltage and high-frequency capacitance-voltage (C-V) measurements are both applied. Remarkably, no measurable current collapse and C-V hysteresis are clearly observed, showing the enhanced interfacial and electric performances of the MOS-HEMT with dielectric engineering of HZO.

1. Introduction

III-nitrides based HEMTs are well-known excellent candidates for high-power, radio-frequency (rf) and high-temperature devices, owing to the high carrier concentration, high carrier mobility and large breakdown voltage [1]. Compared with other III-V heterostructures, the

AlGa_N/Ga_N heterostructures are more advantageous in the HEMTs applications, because of the strong spontaneous and piezoelectric polarization induced 2-dimensional electron-gas (2DEG) at the AlGa_N/Ga_N interface [2]. Nevertheless, the large gate leakage current and gate-lag are still mainly barriers limiting the reliability and properties of AlGa_N/Ga_N HEMTs in high-power, rf, and high-temperature

* Corresponding author. CAS Center for Excellence in Nanoscience, Beijing Key Laboratory of Micro-nano Energy and Sensor, Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing, 100083, China.

** Corresponding author. CAS Center for Excellence in Nanoscience, Beijing Key Laboratory of Micro-nano Energy and Sensor, Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing, 100083, China.

*** Corresponding author. CAS Center for Excellence in Nanoscience, Beijing Key Laboratory of Micro-nano Energy and Sensor, Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing, 100083, China.

E-mail addresses: huaqilin@binn.cas.cn (Q. Hua), huweiguo@binn.cas.cn (W. Hu), zhong.wang@mse.gatech.edu (Z.L. Wang).

<https://doi.org/10.1016/j.nanoen.2019.104361>

Received 4 September 2019; Received in revised form 27 November 2019; Accepted 2 December 2019

Available online 6 December 2019

2211-2855/© 2019 Elsevier Ltd. All rights reserved.

applications [3,4]. These problems are mainly caused by the relatively low-height Schottky barrier formed in the conventional HEMTs which is near about 1 eV, and the surface states within the gate-drain area filled by the electrons emitted from the reverse-biased gate [5]. Due to the large leakage current of conventional AlGaIn/GaN HEMTs, not only the breakdown field but also the power-added efficiency decrease while the noise increasing [6]. Recently, a large number of studies have reported the use of metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) structures to suppress gate leakage current and obtain significant pinch-off characteristics [7]. The gate dielectrics such as SiO₂ [8], Si₃N₄ [9], Ga₂O₃ [10], and Al₂O₃ [11] have also been used in the nitride-HEMTs to form the more effective MOS structure. The gate leakage current is obviously reduced, and the breakdown field is enhanced. Since the deposition of an extra gate dielectric and the formation of a new oxide/AlGaIn interface, it also presents a new challenge that introducing the interface-related imperfections which leading to a gate-lag deteriorate [12]. The gate-lag is manifested as a drop of the pulsed drain current when compared to that of the DC regime. This phenomenon can be described by analyzing the changes of the drain parasitic resistance with dynamic measurements. The drain current collapses seriously limit the high temperature stability and switching performance of the devices, owing to the relatively slow filling and emptying of the interface states [13]. Therefore, it is suggested that a high quality gate dielectric/AlGaIn interface formed in the dielectric engineering is very necessary for the AlGaIn/GaN MOS-HEMTs in fast-switching, high-power applications. However, dielectric engineering increases the separation from gate electrode to the channel, which inevitably decreases the device transconductance (g_m). Recently, high- κ insulating materials such as HfO₂ ($\kappa_{ox} \sim 25$) [14], ZrO₂ ($\kappa_{ox} \sim 30$) [15,16] have been used in the AlGaIn/GaN MOS-HEMTs to improve stability and transport performance of the devices, because the larger dielectric permittivity can be converted to a more efficient gate modulation [17]. Compared to conventional low- κ gate dielectrics, high- κ gate dielectrics can achieve the same equivalent oxidized layer thickness with a thicker geometric thickness, which can more effectively reduce the losses of the device transconductance. As an emerging high- κ gate dielectric material, HfO₂ is attracting much attention in the MOS field-effect transistors applications [18]. However, the main barrier is still existed because it is hard to form a thermodynamically stable and high-quality insulating layer on the AlGaIn/GaN heterostructures, which reduces the interface state density and obtains a good interfacial layer comparable to the SiO₂/Si interface [19]. To date, few papers have reported the use of Hf ternary compounds (e.g., HfAlO_x, and HfSiO_x) as the gate dielectric layer in AlGaIn/GaN HEMTs, to improve the thermal stability of the devices [20–22]. Those devices with high- κ dielectric layers have significantly reduced gate leakage current, but do not show the pronounced enhancement on the output performances.

In this paper, we present AlGaIn/GaN HEMT with dielectric engineering of HZO which is fabricated by incorporating Zr into HfO₂. The as-prepared HZO dielectric layer could have a larger dielectric constant and a relatively better interface properties when compared to that of HfO₂, representing a better dielectric performance [23,24]. Furthermore, we fabricated three types devices, i.e., conventional unpassivated HEMT (conv. HEMT), HfO₂ MOS-HEMT and HZO MOS-HEMT, and systematically investigated the interface properties and output performances in different device configurations. For the HZO MOS-HEMT, not only the saturation current density has been significantly improved, but also a desired interface is simultaneously obtained. It significantly reduces the gate leakage and the current collapse with an excellent output performance. Compared with the high- κ gate dielectric HfO₂ based device, HZO MOS-HEMT also shows enhanced performances in the proposed aspects, which indicates a good prospect for the application of HZO as a gate dielectric.

2. Device structure and fabrication

Fig. 1(a) schematically shows the stack layers of the HZO MOS-HEMTs. The epitaxial layers were synthesized on 4-inch silicon (111) substrate by using metal-organic chemical vapor deposition (MOCVD) with a 2DEG density of $8.5 \times 10^{12} \sim 1.1 \times 10^{13} \text{ cm}^{-2}$ and a carrier mobility of 1850–2010 $\text{cm}^2/\text{V}\cdot\text{s}$. The heterostructure is composed of an AlN/Al_xGa_{1-x}N buffer layer of 3.5–4 μm , a GaN channel layer of 0.4–0.6 μm , an AlN interlayer of 1 nm, an Al_{0.3}Ga_{0.7}N barrier layer of 40 nm and a GaN cap layer of 2 nm. The device fabrication process started with mesa isolation which was implemented by a high power inductively coupled plasma (ICP) etching with Ar/BCl₃/Cl₂ (5/15/30 sccm). The size of an individual device was 24 $\mu\text{m} \times 32 \mu\text{m}$. Then, the Ohmic contacts with Ti/Al/Ni/Au (20/120/45/55 nm) were formed through electron beam deposition and rapid thermal annealing (RTA) at 850 °C for 30 s in N₂ atmosphere. Moreover, a 20 nm thick HZO or HfO₂ was deposited at 200 °C by atomic layer deposition (ALD), and followed by RTA at 600 °C for 30 s in N₂ atmosphere to form the gate dielectric layer. Finally, the Schottky gate metallization was fabricated by the deposition of Ni/Au (80/50 nm). The device without the dielectric layer as the control sample was also prepared by the same process. All the devices with a gate length L_G of 5 μm , a gate width of 24 μm . The gate to source distance L_{GS} and gate to drain distance L_{GD} were 7 μm and 10 μm , respectively. The I - V characteristic of the devices shows Ohmic contacts at drain/source electrodes, as shown in the inset of Fig. 1(a). Fig. 1(b) shows a scanning electron microscopy (SEM) image of an individual HZO MOS-HEMT device. The cross-sectional scanning transmission electron microscope (STEM) image (Fig. 1(c)) is presented to characterize the stack layers and the corresponding thickness which shows that the results are well consistent with our designs. The high-resolution transmission electron microscope (HRTEM) images in Fig. 1(d and e) indicate sharp interfaces of the AlGaIn/GaN and AlGaIn/HZO without obvious defects. Through the HRTEM image of HZO in Fig. 1(e), we can see the dielectric is polycrystalline after the RTA treatment. The energy-dispersive X-ray spectroscopy (EDX) elemental mapping of HZO MOS-HEMT (Fig. 1(f)) clearly shows the distributions of Ga, N, Al, Hf, Zr and O elements, confirming with the stack layers as shown in Fig. 1(c). The band diagram of the fabricated HZO MOS-HEMT at a positive gate-source bias was illustrated in Fig. 1(g). Due to the strong piezoelectric polarization effect, a high density of 2DEG was induced at the AlGaIn/GaN interface. Based on the X-ray photoelectron spectroscopy (XPS) in Fig. 1(h), the composition of HZO film is found to be Hf 0.48 and Zr 0.52, similar to the previous reported [25]. Fig. 1(i) displayed the X-ray diffraction (XRD) curves of the HZO and the HfO₂ films. It clearly shows that the crystal structure of HfO₂ film is a monoclinic phase, while that of the HZO film is a mixture of tetragonal/orthorhombic phases [23]. Additionally, the tetragonal phase has a higher dielectric constant value ($\kappa \sim 40$ –50) when compared to that of the monoclinic phase ($\kappa \sim 20$). So the dielectric constant values of HZO films could be obviously improved.

3. Results and discussion

The DC output performances (I_{ds} - V_{ds}) of the three-type devices, i.e., conv. HEMT, HfO₂ MOS-HEMT, and HZO MOS-HEMT, are shown in Fig. 2(a–c), respectively. In order to facilitate comparison, the practically measured current data has already been converted into gate-width per millimeter [26]. Owing to the high gate to source leakage current, gate voltage of the conv. HEMT can be only applied to +1 V at the optimal working condition, while that of the HfO₂ MOS-HEMT can be applied to +4 V. Impressively, for HZO MOS-HEMT, the gate voltage bias can even reach +6 V at the optimal working condition, which indicates a better stability at higher positive voltages of HZO MOS-HEMTs when compared to the MOS-HEMTs with common high permittivity gate dielectrics or unpassivated HEMTs. Furthermore, the current collapse and gate leakage problems are both obviously reduced by using the dielectric of HfO₂ or HZO. As shown in Fig. 2(d), the maximum output

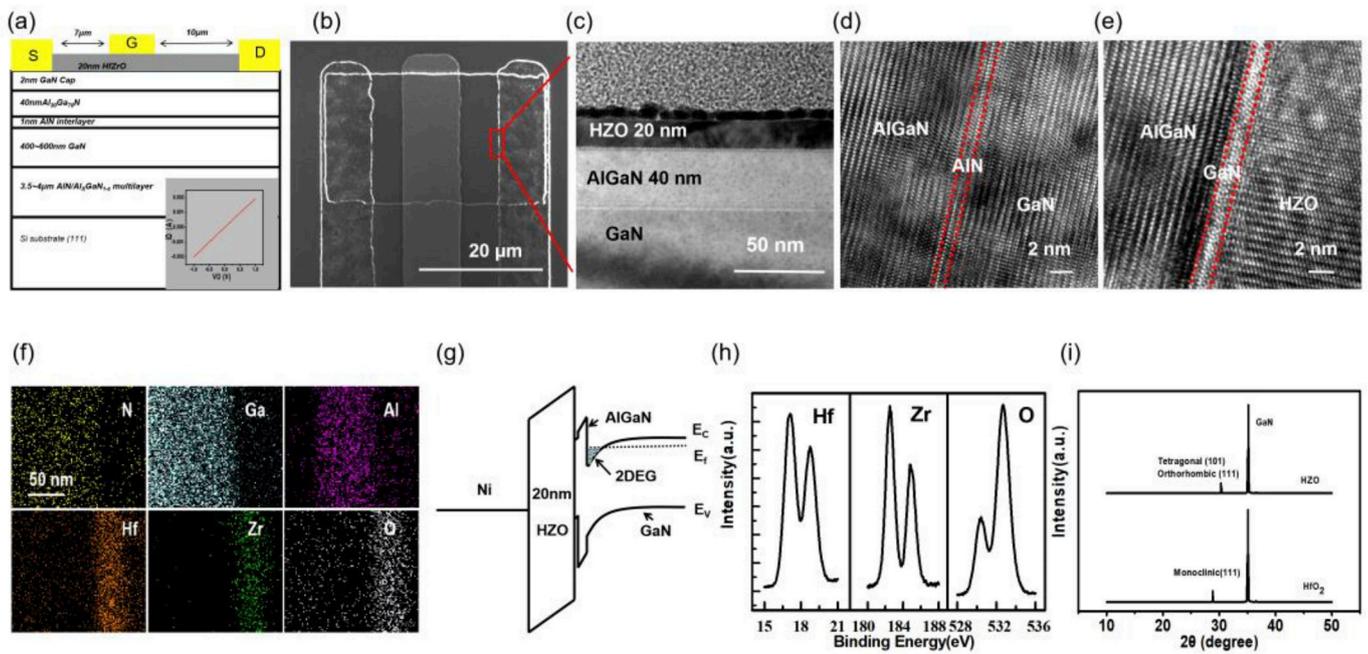


Fig. 1. (a) The cross-section schematic of the HZO MOS-HEMTs with a gate length L_G of 5 μm and gate to source and drain distance of 7 μm and 10 μm , respectively. (b) The scanning electron microscopy (SEM) image of an individual fabricated device. (c) The scanning transmission electron microscope (STEM) image of selected area marked by the red square in (b). The corresponding high-resolution transmission electron microscope (HRTEM) images of AlGaN/AiN/GaN (d) and HZO/GaN/AlGaN (e) interfaces. (f) The energy-dispersive X-ray (EDX) spectroscopy elemental mapping of HZO MOS-HEMT, including the elements of N, Ga, Al, Hf, Zr, and O. (g) The band diagram of the fabricated HZO MOS-HEMT at a positive gate-source bias. (h) The X-ray photoelectron spectroscopy (XPS) analysis of the HZO film. (i) XRD curves of the HZO and the HfO_2 films.

drain current density ($I_{d, \text{max}}$) of the HfO_2 MOS-HEMT and the HZO MOS-HEMT at a positive gate bias of +4 V and +6 V are 640 mA/mm and 705 mA/mm, respectively, while that of the conv. HEMT is only 457 mA/mm at a positive gate bias of +1 V. Obviously, the current density shows an increase by 40% and 54% for the HfO_2 and HZO passivated devices, respectively. It reveals that the MOS-HEMT with HZO dielectric layer exhibits a more effective capability to enhance the device output performances. Normally, the improvement of the saturated drain current density in MOS-HEMTs can be explained as the suppression of the virtual gate effects after the dielectric layers deposited, i.e., decreasing the resistance within the source to drain area by increasing the concentration of the sheet carrier and reducing the gate depletion region [27]. Additionally, reducing the interface traps density at the interface of metal/AlGaN, resulting in an increased carrier density in the active area, thereby improving the maximum drain current density and 2DEG carrier density of the MOS AlGaN/GaN heterostructures [28]. In addition, the HZO film has a larger dielectric constant value and better interface properties. Thereby, the gate controllability of 2DEG channel and the suppression of the virtual gate effect have been increased which can significantly reduce the surface states density and the depletion of electron in the 2DEG channel [29]. So that the output performance of HZO MOS-HEMT is better than that of the HfO_2 MOS-HEMT.

The transfer characteristics of the conv. HEMT, HfO_2 MOS-HEMTs, and HZO MOS-HEMTs are shown in Fig. 3(a–c), respectively. As shown, the threshold voltage (V_{th}) shows negative shifts for the MOS-HEMTs. One reason for the negative shift of the V_{th} is the increased distance between the Schottky contact and the channel by dielectric engineering. It reduces the capacitance of gate-to-channel and weakens the gate control of 2DEG [30]. The other reason is that the newly formed gate dielectric layer would divide the gate partial voltage. Therefore, a larger negative voltage is required to turn the device off. The maximum transconductance ($g_{m, \text{max}}$) of the conv. HEMT measured at V_{ds} of 10 V is 63 mS/mm, as compared to 54 mS/mm and 53 mS/mm for the HZO and HfO_2 passivated MOS-HEMTs, respectively. The reduction of $g_{m, \text{max}}$ in

the MOS-HEMT is inevitable, which is also mainly caused by the larger separation from the Schottky contact to the channel [31]. However, in our devices, the transconductance deterioration is only 14% and 16%, respectively, much smaller than that of the MOS-HEMTs with low- κ gate dielectrics [32], which is benefited from the high dielectric constant of HZO and HfO_2 . Fig. 3(d and e) plots the $I_{\text{ds}, \text{max}}$ and the $g_{m, \text{max}}$ of all three-type devices extracted from Fig. 3(a–c) to more intuitively compare the differences between each other. The HZO MOS-HEMT shows higher stability and performances in this measurement. What is more, the gate voltage swing (GVS), defined as the changes of V_g while the transconductance dropped 10% from the $g_{m, \text{max}}$, is 4.8 V for the HZO MOS-HEMT, 2.2 V for the HfO_2 MOS-HEMT and 2.1 V for the conv. HEMT, as shown in Fig. 3(f). The enhanced GVS linearity is mainly due to the improvement of gate insulation performance and the reduction of surface states in the HZO MOS-HEMT [33]. Higher GVS value demonstrates a better linear performance could be expected in the HZO MOS-HEMT application, by which the phase noise and the intermodulation distortion could be reduced while the dynamic range increasing [31].

The dielectric engineering not only enhanced the output performances and transfer characteristics of the MOS-HEMTs but also obviously improved some other properties of the device. Fig. 4(a) illustrates the $I_{\text{ds}}-V_g$ characteristics of the proposed devices at a constant $V_{\text{ds}} = 10$ V. As is indicated, the minimum subthreshold swing (SS_{min}) of the HZO MOS-HEMT can be scaled down to 85 mV/decade, far smaller than that of the conv. HEMT and HfO_2 MOS-HEMT. It demonstrates that the HZO MOS-HEMT has a lower interface trap density [34]. Furthermore, a high $I_{\text{on}}/I_{\text{off}}$ ratio above 10^6 can also be found in the HZO MOS-HEMT, while that of the HfO_2 MOS-HEMT and conv. HEMT are only 10^2 and $10^{1.5}$. Fig. 4(b) shows the I_g-V_g characteristics of all fabricated devices. From the three curves, all passivated HEMTs exhibit significant reductions of I_g , especially for the HZO MOS-HEMT. When the gate voltage bias applied to -5 V, the gate leakage decreases by eight orders of magnitude compared to the conv. HEMT, and four orders of magnitude lower than

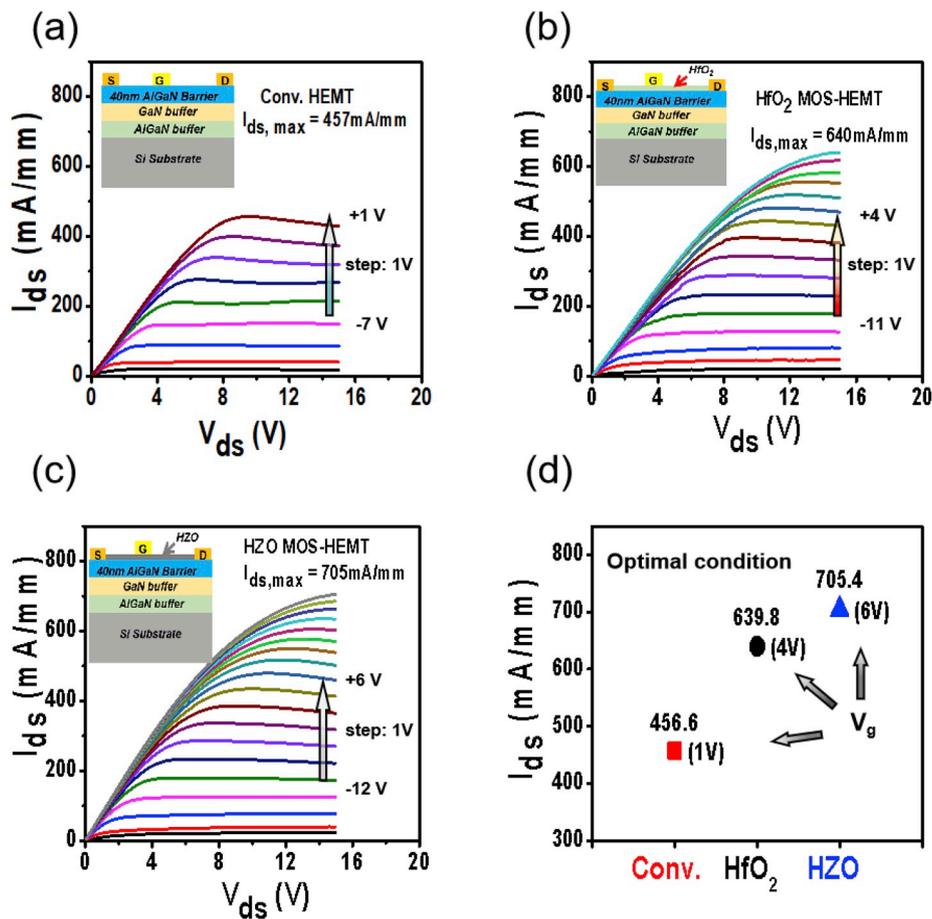


Fig. 2. The DC output performances (I_{ds} - V_{ds}) of the conv. HEMTs (a), HfO₂ MOS-HEMTs (b) and HZO MOS-HEMTs (c). The maximum drain current density ($I_{d, max}$) of fabricated devices measured at optimal working conditions (d).

that of the HfO₂ MOS-HEMT. Much lower gate leakage current means a higher saturated drain current at the positive voltage and a higher breakdown voltage in the device applications [35]. This phenomenon can be explained by two aspects: one reason is that the deposition of dielectric layers can suppress the transport of the charge carrier through the surface states; the other reason mainly causes the considerable reduction of leakage current is the Schottky-barrier formed in conv. HEMTs has been replaced by the more effective MOS structure, which has a larger barrier height [8]. Based on the better interface properties and lower concentration of O₂ vacancies of the HZO dielectric, the HZO MOS-HEMT also exhibits a lower leakage current and a higher I_{on}/I_{off} ratio when compared to the HfO₂ MOS-HEMT [36]. All above data indicates the HZO MOS-HEMT has a higher quality HfZrO_x/AlGaIn interface, which improves the output performances and the passivation properties. In order to further prove this conclusion, we also perform the pulsed I_{ds} - V_{ds} measurements of the three-type devices.

Fig. 5 (a) shows the schematic of the stress voltage applied during the pulsed measurements. The devices are switched by voltage pulses with 1 ms pulse width and 5 ms pulse period. In order to ensure the OFF-state beyond the pulsed plateau, the quiescent bias applied in this pulse measurement is (V_{ds0} , V_{g0}) = (0 V, -12 V). Fig. 5(b-d) show the difference between the DC and pulsed measurement of all three-type devices. As can be seen, the conv. HEMT and HfO₂ MOS-HEMT show significantly current collapse during the measurements. Especially, the HfO₂ MOS-HEMT shows a degradation of 12%, while that of conv. HEMT is only 9%. However, the HZO MOS-HEMT has no obvious degradation of pulsed current, indicating a low surface defect trap density and a high quality of the HZO/AlGaIn interface. It is mainly due to the smaller grains with better equiaxed shape trends, and the

reduction of the equilibrium concentration of O₂ vacancies in the bulk of the grains [24]. In addition, the high-frequency capacitance-voltage (C - V) measurement of the MOS-HEMTs is applied with the voltage bias frequency of 1 MHz, as shown in Fig. 5(e) and (f). Through the forward and reverse sweeps of the C - V hysteresis curve, we can get the drift of the flat-band voltage in the MOS capacitor structure. The drift is mainly owing to traps inside the dielectric layer and electrons trapping effect of the interface states between the dielectric layer and the AlGaIn barrier layer, which can be expressed as [37]:

$$V_{FB} = \Phi_{MS} - \frac{Q_f + Q_{it}(\phi_s) + Q_t}{C_{OX}} \quad (1)$$

Where Φ_{MS} is the difference of the work function between metal and AlGaIn, Q_f and Q_t are the densities of fixed charge and trap charge in the insulated layer, Q_{it} is the surface density of interface state charge, ϕ_s is the semiconductor surface potential. Since Q_f does not change with the scan voltage, the amount of charge corresponding to C - V hysteresis is $Q_{it} + Q_t$, which can be obtained by $V_{FB} \times C_{OX}$. As shown in Fig. 5(e and f), compared with the 30 mV C - V hysteresis of the HfO₂, the extremely low hysteresis and sharp transition of the C - V curve reveal that an effective passivated interface is formed in the HZO MOS-HEMT [38]. From the data in the figures, we also calculated the sum of trap charge density and interface state charge density for the MOS-HEMT. The sum is $1.4 \times 10^{10} \text{ cm}^{-2}/\text{eV}$ and $1.1 \times 10^9 \text{ cm}^{-2}/\text{eV}$ for the HfO₂ MOS-HEMT and HZO MOS-HEMT, respectively, demonstrating a fewer bulk traps in the HZO gate dielectric. It is consistent with the result of the pulse measurement, owing to the improved interface state of the HZO MOS-HEMT.

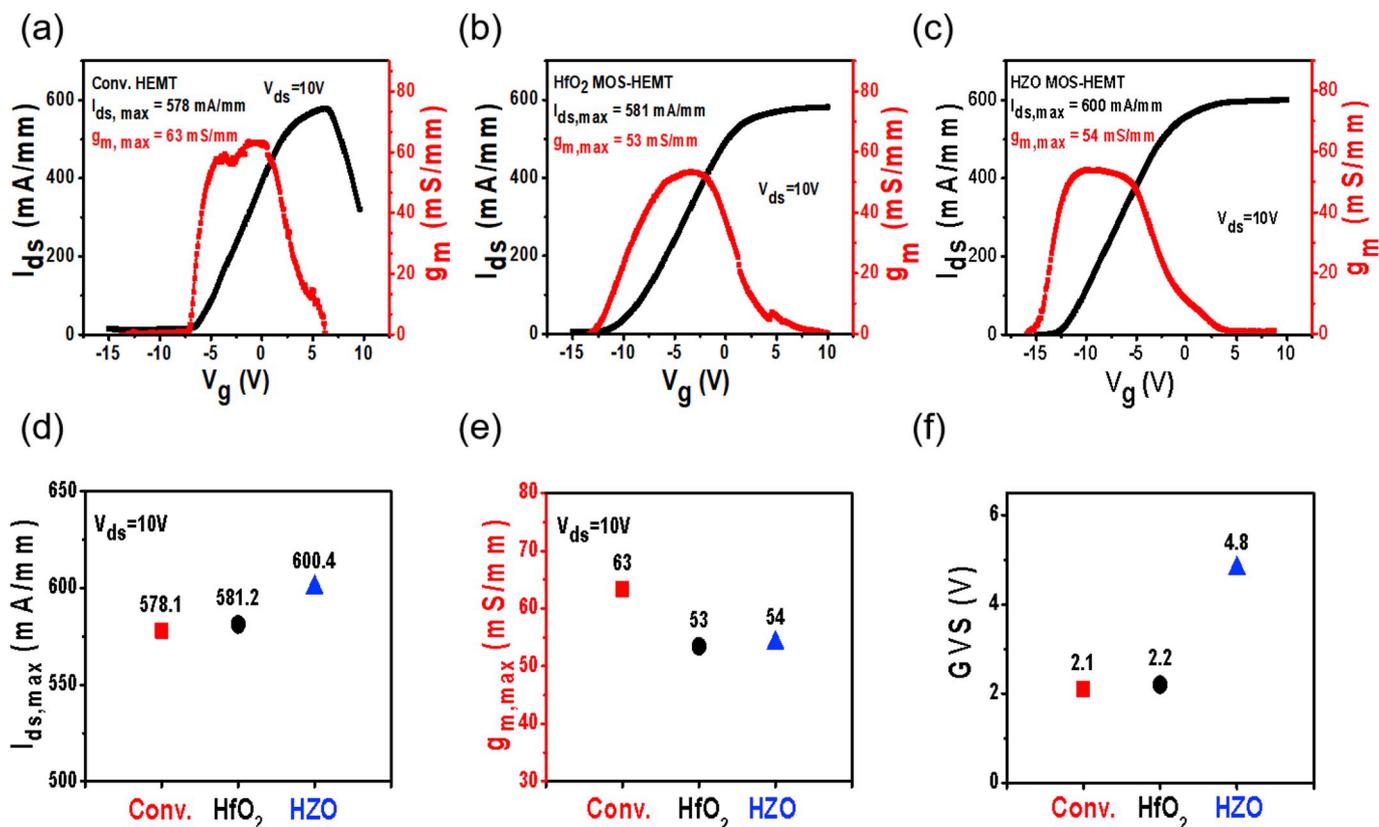


Fig. 3. The transfer characteristics of (a) conv. HEMTs, (b) HfO₂ MOS-HEMTs and (c) HZO MOS-HEMTs measured at V_{ds} = 10 V. The I_{ds,max} (d) and g_{m,max} (e) of the three-type devices. (f) The gate voltage swing (GVS) values of the three-type devices.

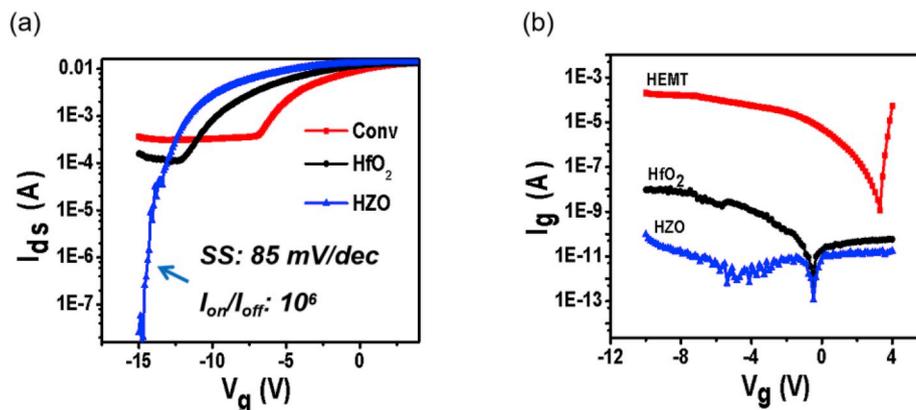


Fig. 4. I_{ds}-V_g characteristics (a) and gate leakage currents characteristics (b) of the conv. unpassivated HEMTs, HfO₂ MOS-HEMTs, and HZO MOS-HEMTs measured at V_{ds} = 10 V.

4. Conclusion

In summary, we successfully fabricated and studied a 20 nm thickness ALD grown HfZrO_x gate dielectric AlGa_n/Ga_n MOS-HEMTs on Si substrates, which shows enhanced interface properties and remarkable output performances. The DC output performances of the proposed devices indicate the superiority of HZO MOS-HEMTs are over the unpassivated HEMTs and the conventional high-κ gate dielectric HfO₂ MOS-HEMTs. At the optimal working conditions, the saturated current density of the HfO₂ and HZO MOS-HEMT increased by 40% and 54%, respectively. Furthermore, the gate leakage of the present device has also been successfully decreased by eight orders of magnitude, which is four orders higher than that of the HfO₂ MOS-HEMT. It suggests that the

HZO insulating layer is more effective as a gate dielectric in the AlGa_n/Ga_n MOS-HEMTs applications to increase saturated drain currents and reduce gate leakage currents. Complete surface passivation has been formed in the gate-drain/source regions which effectively reduces the surface states and helps to resolve the problem of the gate-lag. The result has been proved by following dynamic and C-V measurements, which shows no obvious reduction of the pulse output current or hysteresis for the HZO MOS-HEMT. What is more, the HZO MOS-HEMT also shows more advantages, such as a high I_{on}/I_{off} ratio above 10⁶, an excellent SS value of 85 mV/decade and a higher gate voltage swing of 4.8 V. The higher GVS demonstrates a better linear behavior for the proposed device. Looking forward, the present MOS-HEMT with HZO gate dielectric shows a significantly promising potential for high-frequency, high-

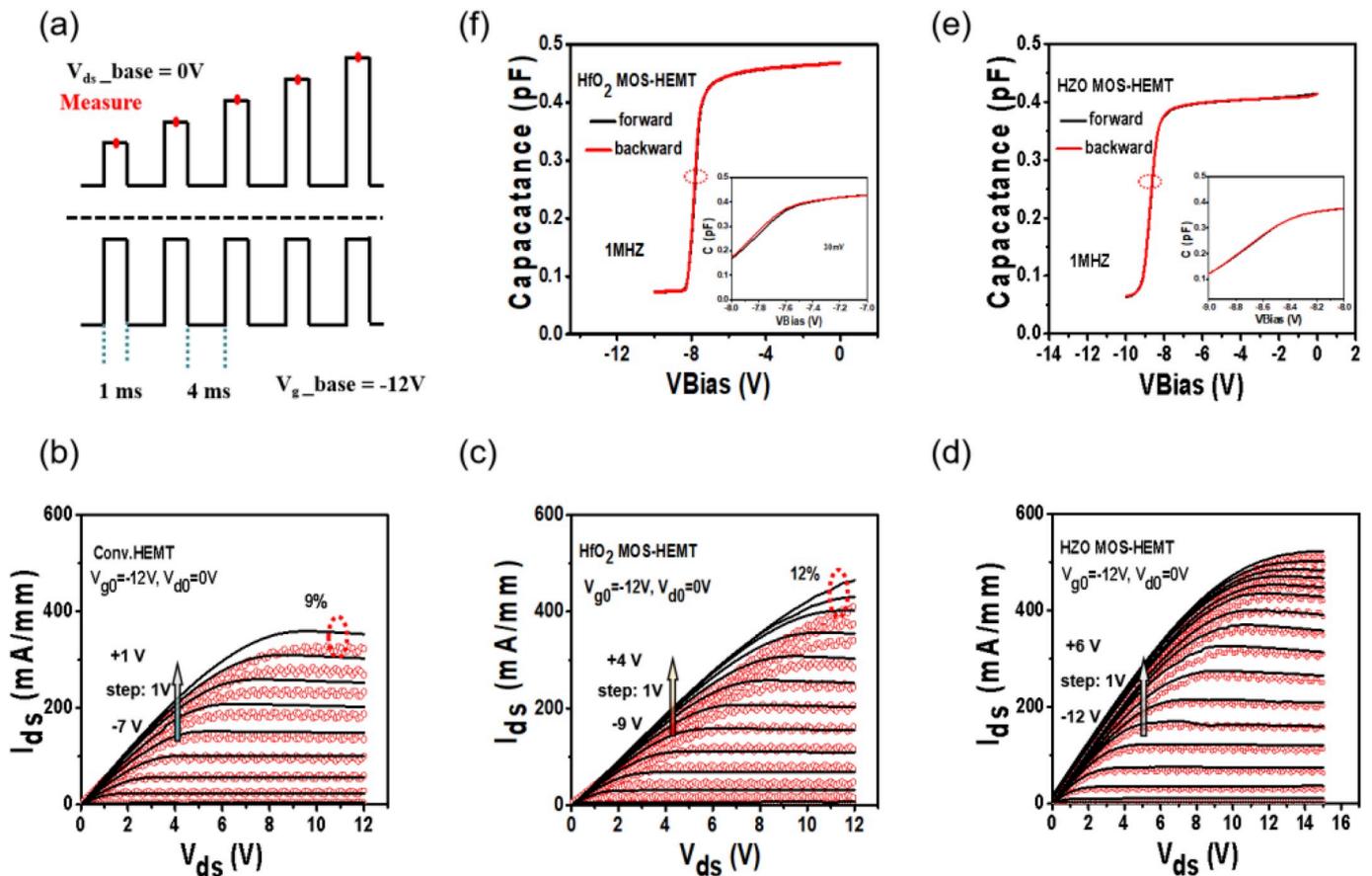


Fig. 5. (a) The schematic of the stress voltage applied during the pulsed measurements, and comparison of the DC and pulsed measurement for (b) conv. HEMTs, (c) HfO₂ MOS-HEMTs and (d) HZO MOS-HEMTs. The high-frequency (1 MHz) capacitance-voltage (C-V) measurements of HZO MOS-HEMT (e) and HfO₂ MOS-HEMTs (f), inset is the magnified view of the area marked by the red circle.

voltage, and high-power applications to reduce the gate leakage and improve the performances.

Acknowledgements

The authors thank for the support from National Key Research and Development Program of China (Grant nos. 2016YFA0202703, 2016YFA0302300, and 2016YFA0200400), National Natural Science Foundation of China (Grant nos. 51432005, 61574018, 61704008, and 61904012), and the “Hundred Talents Program” of the Chinese Academy of Science. R. Liang would like to thank the Research Fund from Beijing Innovation Center for Future Chip.

References

- W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, H. Ohashi, *IEEE Trans. Electron Devices* 50 (2003) 2528–2531.
- S.M. Dinara, S.K. Jana, S. Ghosh, P. Mukhopadhyay, R. Kumar, A. Chakraborty, S. Bhattacharya, D. Biswas, *AIP Adv.* 5 (2015), 047136.
- Y.Z. Yue, Y. Hao, J.C. Zhang, Q. Feng, J.Y. Ni, X.H. Ma, *Chin. Phys. B* 17 (2008) 1405–1409.
- S. Taking, A. Banerjee, H. Zhou, X. Li, A.Z. Khokhar, R. Oxland, I. McGregor, S. Bentley, F. Rahman, I. Thayne, A.M. Dabiran, A.M. Wowchak, B. Cui, E. Wasige, *Electron. Lett.* 46 (2010) 301.
- J. Kuzmik, J.F. Carlin, M. Gonschorek, A. Kostopoulos, G. Konstantinidis, G. Pozzovivo, S. Golka, A. Georgakilas, N. Grandjean, G. Strasser, D. Pogany, *Phys. Status Solidi* 204 (2007) 2019–2022.
- T. Hashizume, S. Ootomo, H. Hasegawa, *Appl. Phys. Lett.* 83 (2003) 2952–2954.
- M.A. Khan, G. Simin, Y. Jinwei, Z. Jianping, A. Koudymov, M.S. Shur, R. Gaska, H. Xuhong, A. Tarakji, *IEEE Trans. Microw. Theory Tech.* 51 (2003) 624–633.
- M.A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, M.S. Shur, *Appl. Phys. Lett.* 77 (2000) 1339–1341.
- X. Hu, A. Koudymov, G. Simin, J. Yang, M.A. Khan, A. Tarakji, M.S. Shur, R. Gaska, *Appl. Phys. Lett.* 79 (2001) 2832–2834.
- C.-T. Lee, H.-W. Chen, H.-Y. Lee, *Appl. Phys. Lett.* 82 (2003) 4304–4306.
- Y. Yue, Y. Hao, Q. Feng, J. Zhang, X. Ma, J. Ni, *Sci. China Ser. E Technol. Sci.* 52 (2008) 2762–2766.
- K. Čičo, K. Huseková, M. Tápajna, D. Gregušová, R. Stoklas, J. Kuzmik, J.F. Carlin, N. Grandjean, D. Pogany, K. Fröhlich, *J. Vac. Sci. Technol. B Nanotechnol. Microelectr.: Mater. Process. Meas. Phenomen.* 29 (2011), 01A808.
- R. Veturly, N.Q. Zhang, S. Keller, U.K. Mishra, *IEEE Trans. Electron Devices* 48 (2001) 560–566.
- C. Liu, E.F. Chor, L.S. Tan, *Semicond. Sci. Technol.* 22 (2007) 522–527.
- Y. Han, S. Klenov, D. Hansen, P.J. No, J.S. Speck, *J. Vac. Sci. Technol. B, Microelectr. nanometer. struct.: Process. Meas. Phenomen. Off. J. Am. Vac. Soc.* 24 (2006) 575–581.
- J. Kuzmik, G. Konstantinidis, S. Harasek, Š. Haščik, E. Bertagnolli, A. Georgakilas, D. Pogany, *Semicond. Sci. Technol.* 19 (2004) 1364–1368.
- C. Liu, E.F. Chor, L.S. Tan, *Appl. Phys. Lett.* 88 (2006) 173504.
- E.P.N. Gusev, V. Narayanan, M.M.V. Frank, *IBM J. Res. Dev.* 50 (2006) 387–410.
- Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng, L. Liu, *IEEE Electron. Device Lett.* 29 (2008) 838–840.
- A. Colón, J. Shi, *Solid State Electron.* 99 (2014) 25–30.
- C. Kirkpatrick, B. Lee, X. Yang, V. Misra, *Phys. Status Solidi* 8 (2011) 2445–2447.
- S. Li, Q. Hu, X. Wang, T. Li, X. Li, Y. Wu, *IEEE Electron. Device Lett.* 40 (2019) 295–298.
- D.-Y. Cho, H.-S. Jung, C.S. Hwang, *Phys. Rev. B* 82 (2010).
- D.H. Triyoso, R.I. Hegde, J.K. Schaeffer, D. Roan, P.J. Tobin, S.B. Samavedam, B. E. White, R. Gregory, X.D. Wang, *Appl. Phys. Lett.* 88 (2006) 222901.
- H.-C. Chiu, C.-H. Wu, J.-F. Chi, F.-T. Chien, *Microelectron. Reliab.* 54 (2014) 1282–1287.
- D. Shahrijeri, J. Nah, B. Hekmatshoar, T. Akyol, M. Ramon, E. Tutuc, S. K. Banerjee, *Appl. Phys. Lett.* 97 (2010) 213506.
- G. Heidelberger, J. Bernát, A. Fox, M. Marso, H. Lüth, D. Gregušová, P. Kordoš, *Phys. Status Solidi* 203 (2006) 1876–1881.
- W. Wang, J. Derluyn, M. Germain, M. Leys, S. Degroote, D. Schreurs, G. Borghs, *Jpn. J. Appl. Phys.* 45 (2006) L224–L226.
- M. Marso, G. Heidelberger, K.M. Indlekofer, J. Bernat, A. Fox, P. Kordoš, H. Luth, *IEEE Trans. Electron Devices* 53 (2006) 1517–1523.
- C. Liu, E.F. Chor, L.S. Tan, *Appl. Phys. Lett.* 88 (2006) 173504.
- M.A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, M.S. Shur, *IEEE Electron. Device Lett.* 21 (2000) 63–65.

- [32] V. Adivarahan, M. Gaevski, A. Koudymov, J. Yang, G. Simin, M.A. Khan, *IEEE Electron. Device Lett.* 28 (2007) 192–194.
- [33] B.-Y. Chou, C.-S. Lee, C.-L. Yang, W.-C. Hsu, H.-Y. Liu, M.-H. Chiang, W.-C. Sun, S.-Y. Wei, S.-M. Yu, *IEEE Electron. Device Lett.* 35 (2014) 1091–1093.
- [34] S. Li, Q. Hu, X. Wang, T. Li, X. Li, Y. Wu, *IEEE Electron. Device Lett.* 40 (2019) 295–298.
- [35] T. Liu, C. Jiang, X. Huang, C. Du, Z. Zhao, L. Jing, X. Li, S. Han, J. Sun, X. Pu, J. Zhai, W. Hu, *Nano Energy* 39 (2017) 53–59.
- [36] M.N.U. Bhuyian, S. Poddar, D. Misra, K. Tapily, R.D. Clark, S. Consiglio, C. S. Wajda, G. Nakamura, G.J. Leusink, *Appl. Phys. Lett.* 106 (2015) 193508.
- [37] E.H. Nicollian, J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, John Wiley & Sons, 2002.
- [38] J.W. Chung, J.C. Roberts, E.L. Piner, T. Palacios, *IEEE Electron. Device Lett.* 29 (2008) 1196–1198.



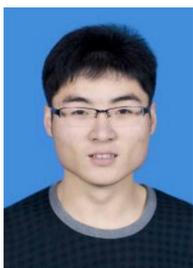
Xiao Cui received his B.S. degree from Xidian University in 2016. He is pursuing his M.S. degree in condensed matter physics at University of Chinese Academy of Sciences (UCAS) since 2017. His research interests focus on GaN-based power devices and the piezotronic effect.



Dr. Renrong Liang received the Ph.D. degree in electronics science and technology from Tsinghua University in 2008. As an Assistant Professor with the Institute of Microelectronics at Tsinghua University, his current research interests are concerned with fabrication and simulation of SiGe and 2D materials-based devices, transport models and optimization of low-power nanoscale MOS devices, such as strained Si MOS-FETs, FinFETs, tunneling FETs and negative capacitance FETs, and device physics.



Prof. Weiguo Hu is a principal investigator at the Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Science (CAS), China. He received his PhD degree from the Institute of Semiconductors, CAS, in 2007. His research focuses on gallium nitride-based piezotronic/piezo-phototronic devices and wearable self-powered nanosystems. He has authored more than 70 peer-reviewed journal articles in these fields.



Weijun Cheng received the B.S. degree in microelectronics from Jilin University, Changchun, China, in 2016. He is currently pursuing the Ph.D. degree in electronic science and technology with the Department of Microelectronics, Tsinghua University, China. His current research interests include tunnel FETs, NCFETs, and IGZO based novel thin-film transistors.



Prof. Zhong Lin (Z L) Wang received his Ph.D. from Arizona State University in physics. He now is the Hightower Chair in Materials Science and Engineering, Regents' Professor, Engineering Distinguished Professor and Director, Center for Nanostructure Characterization, at Georgia Tech. Dr. Wang has made original and innovative contributions to the synthesis, discovery, characterization and understanding of fundamental physical properties of oxide nanobelts and nanowires, as well as applications of nanowires in energy sciences, electronics, optoelectronics and biological science. His discovery and breakthroughs in developing nanogenerators established the principle and technological road map for harvesting mechanical energy from environment and biological systems for powering personal electronics. His research on self-powered nanosystems has inspired the worldwide effort in academia and industry for studying energy for micro-nano-systems, which is now a distinct disciplinary in energy research and future sensor networks. He coined and pioneered the field of piezotronics and piezo-phototronics by introducing piezoelectric potential gated charge transport process in fabricating new electronic and optoelectronic devices.



Dr. Qilin Hua received his B.S degree from Huazhong University of Science and Technology (HUST) in 2010 and Ph.D. degree from University of Chinese Academy of Sciences (UCAS) in 2016. He then joined Tsinghua University. He is currently an associate professor at Beijing Institute of Nanoenergy and Nanosystems (BINN), Chinese Academy of Science (CAS). His research interests include flexible/stretchable electronics, low-dimensional materials, GaN-based piezotronic/piezo-phototronic devices, memristors, and neuromorphic systems.