Wafer-Scale High-Throughput Ordered Arrays of Si and Coaxial $Si/Si_{1-x}Ge_x$ Wires: Fabrication, Characterization, and Photovoltaic Application

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ABSTRACT We have developed a method combining lithography and catalytic etching to fabricate large-area (uniform coverage over an entire 5-in. wafer) arrays of vertically aligned single-crystal Si nanowires with high throughput. Coaxial n-Si/p-SiGe wire arrays are also fabricated by further coating single-crystal epitaxial SiGe layers on the Si wires using ultrahigh vacuum chemical vapor deposition (UHVCVD). This method allows precise control over the diameter, length, density, spacing, orientation, shape, pattern and location of the Si and Si/SiGe nanowire arrays, making it possible to fabricate an array of devices based on rationally designed nanowire arrays. A proposed fabrication mechanism of the etching process is presented. Inspired by the excellent antireflection properties of the Si/SiGe wire arrays, we built solar cells based on the arrays of these wires containing radial junctions, an example of which exhibits an open circuit voltage (V_{oc}) of 650 mV, a short-circuit current density (J_{sc}) of 8.38 mA/cm^2, a fill factor of 0.60, and an energy conversion efficiency (η) of 3.26%. Such a p—n radial structure will have a great potential application for cost-efficient photovoltaic (PV) solar energy conversion.

KEYWORDS: Si wires arrays · radial $Si/Si_{1-x}Ge_x$ wire arrays · single crystal epitaxial growth · PV application

Silicon micro/nanowires (Si wires) are promising candidates for future applications in electronics and photonics since Si-based devices have dominated integrated circuits for many decades. Vertical arrays of Si wires have been especially sought after for many applications, such as nanoimprint masters,[1] vertical field effect transistors,[2−4] Li-ion battery negative electrodes,[5,6] solar cells,[7,8] and even for biochemical cancer molecular detection.[9] Further, arrays of vertical Si wires containing radial junctions attract attention for solar cells because of their ability to decouple the light absorption direction from the direction of charge-carrier collection and light trapping.[10] Vertical Si wires can be synthesized with different mechanisms, such as vapor—liquid—solid (VLS),[11] solid—liquid—solid (SLS),[12] solution—solid—solid,[13] vapor—solid—solid (VSS),[14,15] and oxide-assisted growth (OAG),[16−18] among which the VLS process is the most frequently used approach since this catalyst confined growth has been proven to be an effective method for size and position control. However, these growth mechanisms show some limitations in practice: for example, they generally need high temperatures or high vacuum, complex equipment, and sometimes hazardous Si precursors (such as SiH_4 or $SiCl_4$).

Earlier, we reported a metal-assisted catalytic etching method to fabricate vertical Si wires directly from silicon wafer under mild conditions at low synthetic temperatures in simple equipment with a low cost.[19−22] By combining the catalytic etching with a nanosphere self-assemble method,[23] we fabricated Si wire arrays with controlled diameter, length, and density. However, this process still cannot produce large-scale uniform Si wire arrays, since the ordered self-assembled nanosphere zone is only several micrometers in size. The precise control of the location, pattern, and shape of the arrays has not been realized, either. To obtain high-quality wire arrays for large-scale device applications, we need an approach that can meet the following four requirements. First, the growth has to be performed at a low temperature so that the wires can be integrated with various

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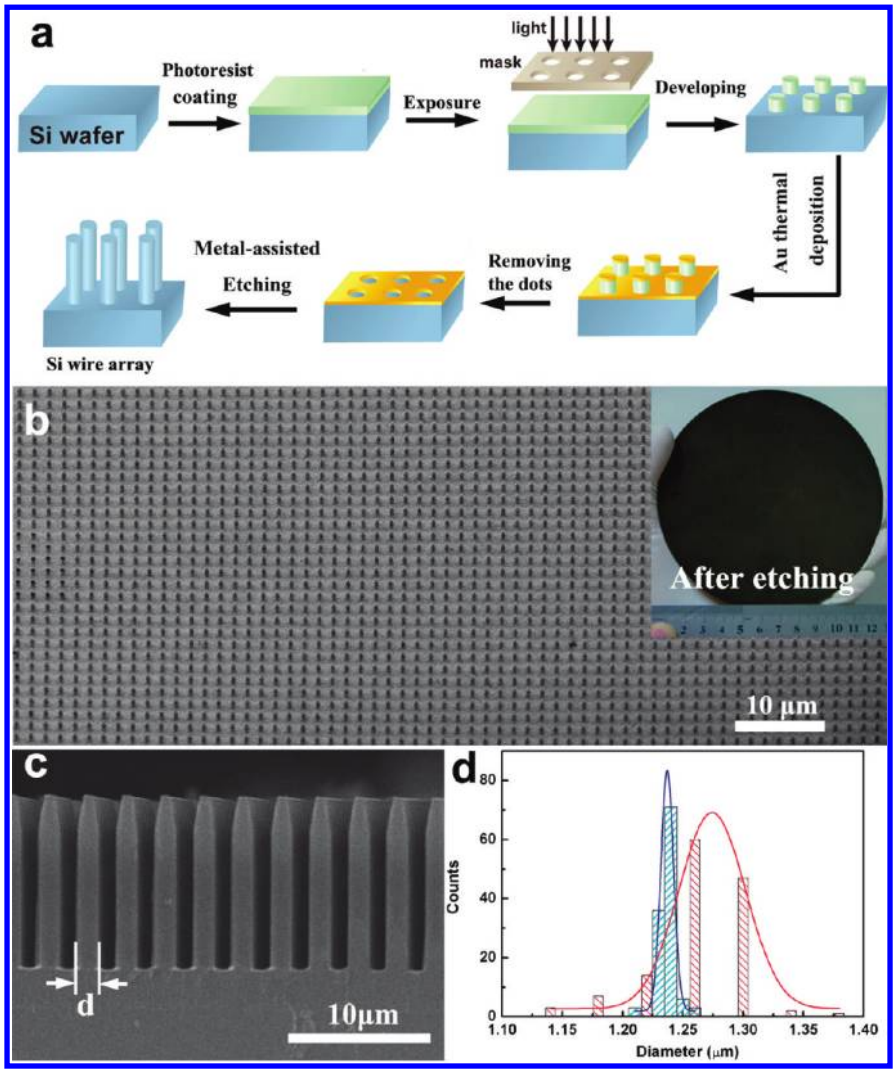

Figure 1. (a) Schematic diagram illustrating the fabrication of Si wire arrays using a combination of lithography and catalytic etching. (b) Top-view scanning electron microscope (SEM) image of a Si wire array. The inset is the optical photograph of a 5 in. Si wafer, which "looks" very black, after the catalytic etching. (c) Cross-section view of a Si wire array by SEM, where "d" indicates a typical position to measure the diameter of a wire. (d) Size distributions of the Si wires in an array and the photoresist dots used in the corresponding lithography. The red and the blue curves correspond to the wires and the photoresist dots, respectively.

substrates. Second, the wires have to be grown rationally following designed patterns with a high degree of control over the size, location, packing manner, dimensionality, uniformity and possibly shape as well as composition/heterostructure. Third, all of these arrays should be fabricated over a large area with a high throughput and a low cost. Finally, the catalyst may need to be eliminated for integration with silicon-based technology.[24] In this paper, we demonstrate an approach that uses a combination of catalytic etching and lithography and can produce large-scale ordered arrays of Si wires with precise control over a wide range of diameters, lengths, spacings, cross-sectional shapes, and locations. Further, radial n-Si/p-SiGe junctions are fabricated on the Si wires by epitaxial growth and these Si/SiGe wire arrays are successfully used to build solar cells, giving energy conversion efficiency up to 3.26%.

RESULTS AND DISCUSSION

Fabrication and Characterization of Si Wire Arrays. Figure 1a shows the main experimental steps in our lithography/catalytic-etching for Si wire arrays. First, an array of photoresist dots with designed diameter, spacing, pattern, and location was obtained on a 5 in. Si wafer by a standard lithography. Then a gold (or silver) film was thermally evaporated onto the Si wafer. After the photoresist dots were removed, a gold film with ordered holes was obtained and the diameters of the holes match those of the photoresist dots. Subsequently, an etching step was conducted to produce Si wires in a mixture of deionized water, HF, and H_2O_2. The Au was then removed using a standard Au etchant. Figure 1(b,c) shows scanning electron microscope (SEM) images of the Si wire arrays. The low-magnification top-view SEM image in Figure 1b clearly shows homogenously distributed Si wires covering a large

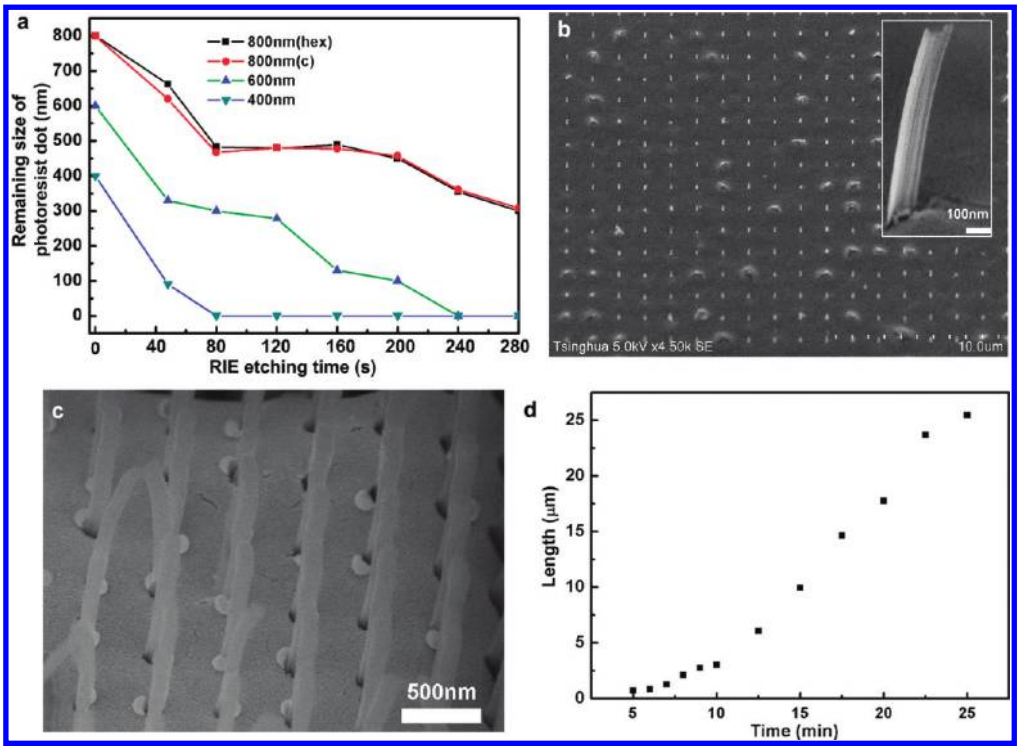

Figure 2. Size and length control of the Si wire arrays. (a) The control of the size of the photoresist dots with RIE, where "hex" and "c" are the hexagonal and the cubic arrangements of the dot arrays, respectively. (b) SEM image of a Si nanowire array with diameter around 100 nm, fabricated with reduced photoresist dots as template. The inset is the close-up of a nanowire. (c) Small-diameter Si nanowire array fabricated by EBL and the catalytic etching. (d) The relationship between the length of the Si wires and the etching time.

area. A cross-sectional view of another Si wire array, in which the Si wires have uniform shape, is shown in Figure 1c. SEM images are used to analyze the size distributions of the Si wires and photoresist dots, and a result is shown in Figure 1d. For this result, the diameter of the photoresist dots was designed to be 1.25 μm with the mask, and the mean diameters of the obtained photoresist dots and Si wires were 1.24 and 1.27 μm, respectively. The deviation between them was only 2%. This indicates that we can design and fabricate Si wires with desired diameters by controlling the size of photoresist dots directly and precisely. Owing to the restriction from the resolution of the lithography instrument, we can only obtain photoresist dots with diameters over 400 nm in this work. To decrease the diameter of the Si wires, three approaches can be taken: (I) With the use of a lithography instrument with higher resolution, such as deep UV lithography[25,26] or extreme ultraviolet lithography (EUL),[27−29] photoresist dots less than 100 nm can be obtained. Even more, Intel has achieved 45 nm on its commercial CPU productions (called "Penryn"). (II) A reactive ion etching (RIE) treatment can be used for shrinking the size of prepared photoresist dots, as shown in Figure 2a. In the work shown by Figure 2a, four kinds of photoresist dot arrays with different diameters were designed: 800 nm (hexagonal patterned), 800 nm (cubic patterned), 600 nm (cubic patterned), and 400 nm (cubic patterned). After RIE was applied on these dot arrays, we obtained photoresist dots with diameters from 50 to 800 nm, and the diameter depended on the RIE time. Using these RIE reduced photoresist dots as template, Si wires with diameters down to 100 nm were fabricated easily, as shown in Figure 2b. Deep etching of the photoresist dots (*e.g.*, from 600 to 50 nm) produces a sawtooth and unregular shape of the photoresist dots; this results in a zigzag surface and unregular shape of the Si nanowires which are prepared using such a template. The RIE treatment is a very useful strategy if you want to obtain small diameter Si nanowires but you only have poor resolution lithography systems. (III) Electron-beam lithography (EBL) combined with the catalytic etching can define features down to sub-10 nm,[30] and a result made by EBL is shown in Figure 2c. But the cost of EBL is very high and the throughput is low. The length of the Si wires can also be well controlled by the duration of the catalytic etching. The relationship between the length and the etching time is shown in Figure 2d, indicating that Si wires with height varying from 1 to 25 μm were obtained by varying the etching time of our process from 1 to 25 min. Nanowires with aspect ratios as large as 30:1 can be easily fabricated by our method.

Mechanisms for the Metal-Assisted Etching Process. Mechanism is very important to the metal assisted etching process; however, due to difficulties in observing the

in situ etching process, there are no explicit experimental results to support a mechanism. By tracking the catalyst particles, several mechanisms have been proposed. Two typical models of them are shown in Figure 3a−c.

The mechanism shown by Figure 3a,b is proposed by our group and states that chemical or electrochemical reactions occur preferentially near the noble metal (such as Au and Ag, here we take Au as an example). That is to say, the Au film catalyzes the etching of Si beneath it and then the vertical sinking of the Au film etches away the Si beneath it. Finally, the remnant Si forms a wire array.[21,23,31]

It is well accepted that the H_2O_2 is reduced at the metal (cathode reaction):

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \quad (1)$$

while a mixed reaction composed of divalent and tetravalent dissolution for the dissolution of Si in metal-assisted chemical etching (anode reaction) is[32]

$$Si + 6HF + nh^+ \rightarrow H_2SiF_6 + nH^+ + \frac{4-n}{2}H_2\uparrow \quad (2)$$

and the overall reaction is

$$Si + \frac{n}{2}2H_2O_2 + 6HF \rightarrow H_2SiF_6 + nH_2O + \frac{4-n}{2}H_2\uparrow \quad (3)$$

Hole injection is well-recognized as a charge transfer process for metal-assisted chemical etching of Si since charge transfer is necessary for the electrooxidation and dissolution of Si. During the etching process, the noble metal acts as a microscopic cathode on which the reduction of the oxidant occurs (cathode reaction 1). The generated holes are then injected into the Si substrate in contact with the noble metal. Then, the Si atoms under the noble metal are oxidized due to the hole injection and dissolved by HF (anode reaction 2).

The other mechanism assumes that those metal particles or films (Ag or Au, *etc.*) protect the Si underneath from being etched, as shown in Figure 3c,[33−37] since metal particles were observed on the top of the Si nanowires. No doubt the etching of Si by HF/H_2O_2 does occur if the metal particles or films only act as a protector, but the etching rate is lower than 10 nm per hour in an etchant (which is far slower than the metal-assisted etching 1 μm per minute) with a concentration of H_2O_2 much higher than that used in metal-assisted chemical etching.[38]

As a result, clarification of the etching mechanism with obvious and strong evidence is very important for the research and application of the metal-assisted etching process. Figure 3d shows inhomogeneous etching at the beginning period. The different etching speeds can be attributed to the variations of the local chemical environment, such as temperature and concentration of the etching solution. The left part in Figure 3d had no wires under a slower etching speed,

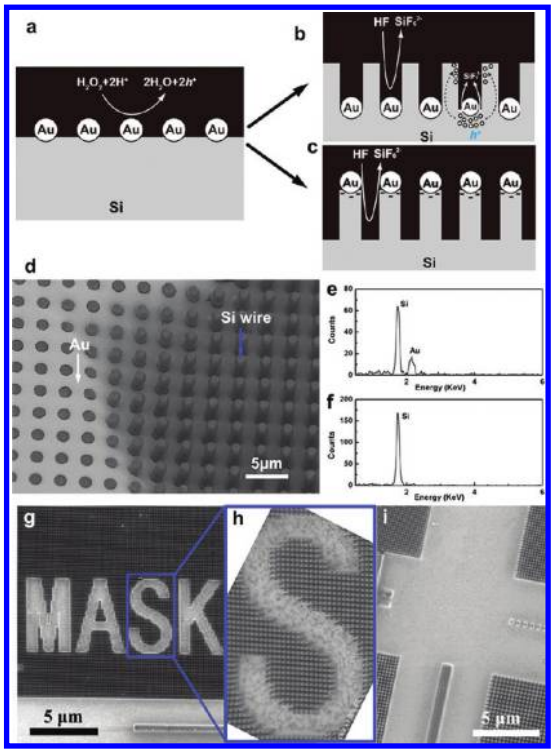

Figure 3. (a−c) Two proposed fabrication mechanisms of the catalytic etching. (d) SEM image of a specific area at the beginning period of the etching process, showing an inhomogeneous etching speed between different areas. (e,f) The EDX spectra corresponding to the Au film and Si wire in panel d, respectively. (g−i) SEM images showing the compatibility of our process with complementary metal oxide semiconductor (CMOS) technology to make patterned and designed Si wire arrays.

while the Si wires appeared at the right part under a faster etching speed. According to the energy dispersive X-ray (EDX) spectra shown in Figure 3e,f, it is obvious that the sinking Au film catalyzes the etching of Si beneath it, and there is no gold remaining on the top of the as-prepared Si wires. That is to say, during the etching process, the silicon beneath the Au film was gradually etched away and the remnant silicon formed a wire array. The above results support the mechanism that the catalyst particles or films only catalyze the etching of Si in contact with them and do not prevent the Si from being etched.

In summary, the overall etching process is suggested here: first, the oxidant (such as H_2O_2) is preferentially catalytically reduced at the surface of the metal particle (cathode reaction 1). Second, the holes generated due to the reduction of the oxidant in the first step diffuse through the metal particles and are injected into the Si that is in contact with the metal. Third, Si is oxidized and dissolved (anode reaction 2) at the interface of the Si and the metal, while the byproduct H_2SiF_6 diffuses into the solution. Fourth, the holes diffuse from the Si in contact with the metal to the side wall or the metal off area if the holes consumption rate is lower than the injection rate. Accordingly, the side walls

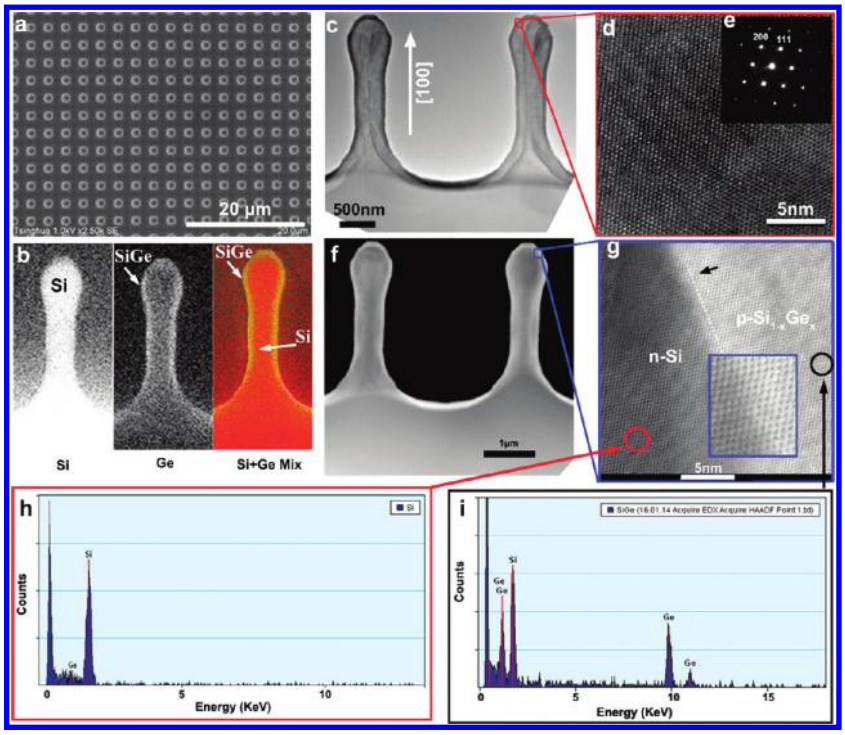

Figure 4. Coaxial n-Si/p-SiGe wire arrays. (a) Top-view SEM image of an array. (b) EDX mapping of an individual Si/SiGe wire under SEM, indicating a full coverage of SiGe layer on the Si wire. The inner layer (red) is the n-Si core, and the outer layer (gold color) is the p-SiGe layer. (c) Low-magnification bright field TEM image of the Si/SiGe junction structure, whose growth direction is [100]. (d) High-resolution TEM image of the junction structure, showing the interface between the n-Si core and the p-SiGe shell layer. (e) Selected-area electron diffraction (SAED) pattern taken from a Si/SiGe junction wire. (f,g) STEM images corresponding to panel c, showing a clear and perfect interface between the Si core and the SiGe shell. (h,i) EDX spectra acquired from the Si core and the SiGe layer, respectively, under the STEM mode.

maybe etched due to the injection of holes, getting a nonsmooth surface of the as-prepared Si nanowires. Finally, the metal particles gradually sink and etch away the Si in contact with them, and the remnant silicon forms a wire array.

Based on the etching mechanism, our method has a good compatibility with the large scale complementary metal oxide semiconductor (CMOS) technology. Through a proper layout design, we can obtain Si wires in selected areas and keep other areas unchanged, as shown in Figures 3g–i, where the pattern of the Si wires composed a word "MASK".

Fabrication and Characterization of Radial n–p Si/Si$_{1-x}$Ge$_x$ Wire Structures. Arrays of Si wires have numerous applications. Here we demonstrate their performance as solar cells. Compared to axial p–n junctions reported previously by us,[39,40] radial p–n junctions have more advantages, such as larger p–n junction areas, low bulk recombination, and good carrier collection. Nevertheless, solar cells based on radial junction wire arrays still face critical challenges such as large surface recombination and interface recombination losses. In the past, shell layers were always polycrystal materials.[41–43] There is, however, little work reported on single crystal epitaxial p–n coaxial silicon wire structures up to date.[44,45] In this work, we report single crystal epitaxial radial n–p Si/Si$_{1-x}$Ge$_x$ (x = 0 and 0.17) wire structures, by epitaxial coating a single crystal SiGe layer on the as-prepared Si wire arrays, which could decrease the losses due to the interface and intercrystalline recombinations.

Figure 4a is the SEM image of an as-prepared coaxial Si/SiGe wire array. Similar to Si wires, the coaxial Si/SiGe wires can be controlled in terms of diameter, length, spacing, doping, and pattern. An SEM EDX mapping of an individual Si/SiGe wire is shown in Figure 4b, indicating that the whole outer surface of the Si wire is coated by a SiGe layer with an average thickness of about 60–70 nm. Figure 4c is a low-magnification TEM image, together with the high-resolution TEM image in Figure 4d and the selected-area electron diffraction (SAED) pattern in Figure 4e, showing that the axis direction of the Si/SiGe wire is [100]. Figure 4d indicates that the epitaxial growth between the Si core and the SiGe shell is good and no obvious interface can be found. Scanning transmission electron microscopy (STEM) images are listed as Figure 4f,g for the investigation of the interface. In the high-magnification STEM image (Figure 4g), a perfect interface between n-Si and p-SiGe can be observed, and the epitaxial SiGe layer has high quality. EDX spectra acquired under the STEM mode indicate that Ge exists not in the Si core (Figure 4h) but in the SiGe layer (Figure 4i).

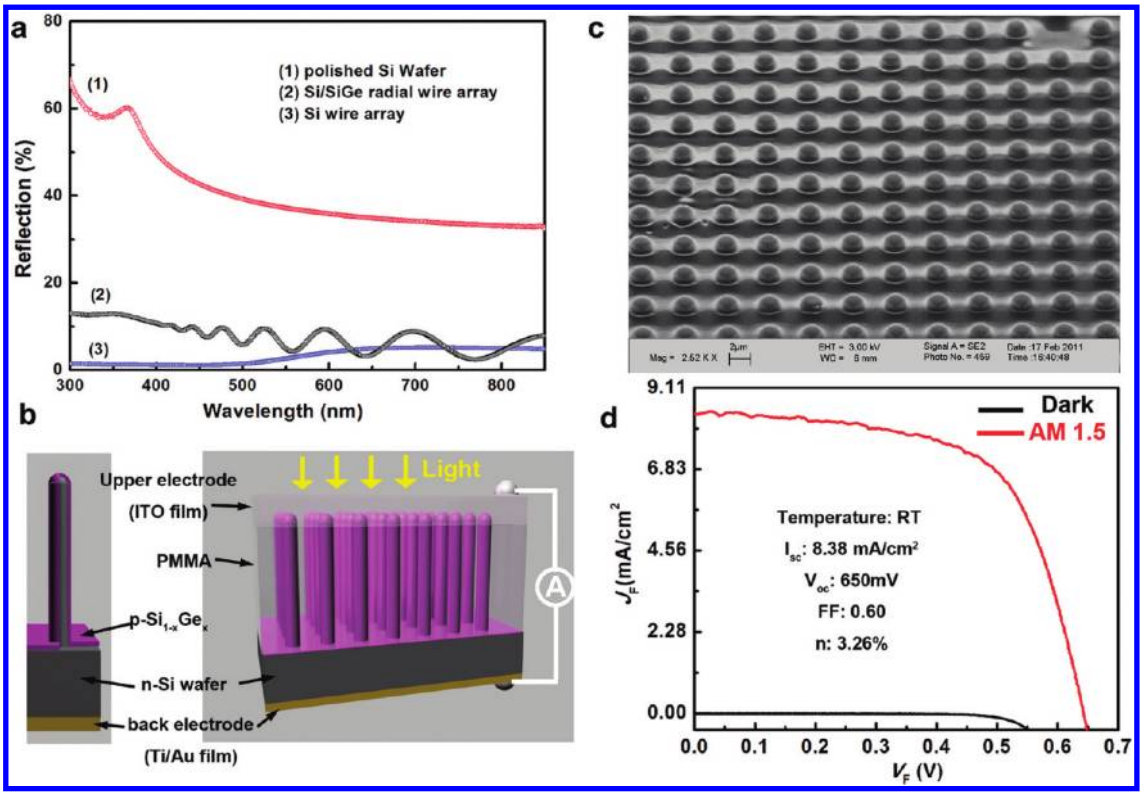

Figure 5. (a) Reflectance (*R*) as a function of wavelength. Red curve, polished silicon; blue curve, array of Si wires with 600 nm in diameter and ~4 μm in length; black curve, Si/Si$_{1-x}$Ge$_x$ radial wire array with the n-Si cores having 600 nm in diameter and ~4 μm in length and the 70 nm p-SiGe shells (x = 0.17 here). (b) Design overview of the Si/SiGe radial wire array solar cells. (c) Tilt-view SEM image of a Si/SiGe wire array wrapped with a thick layer of PMMA, where only the tips of the wires are exposed. (d) *I*−*V* curves for a Si/SiGe solar cell in the dark and under the AM1.5 illumination.

The as-synthesized Si and Si/SiGe wire arrays look very "black", as shown in the inset of Figure 1b. This implies their potentially high antireflection property. We carried out absolute hemispherical measurements with an integrating sphere (Hitachi U-4001 UV−vis spectrophotometer) on the wire arrays. Figure 5a shows the reflectance of an as-synthesized Si wire array, a Si/SiGe wire array, and a polished silicon wafer. The reflectance of the Si and radial Si/SiGe wire arrays are both less than 10%, drastically decreased relative to that of the polished silicon wafer in the visible light region. The regular multiple peaks in the reflection spectrum of the Si/SiGe wire array were caused by the thin film interference between the SiGe shells and the Si cores.[46]

Radial n-p Si/Si$_{1-x}$Ge$_x$ Wire-Based Solar Cells. Inspired by the good antireflection property of the Si/SiGe wire arrays, we built solar cells based on the wires with the radial junctions. After the growth of the SiGe layer onto the Si wire array on a Si substrate, a layer of Ti/Au (5 nm/50 nm) was deposited by electron beam evaporation on the back of the n-Si substrate as the back electrode. Then a relatively thick layer of PMMA (Microchem) was carefully spun onto the substrate to bury the wire array. After this, oxygen plasma was applied to etch away the top part of the PMMA and to expose the tips of the wires. Then, a 200-nm layer of ITO was sputtered as the top common electrode of the solar cell. Figure 5 panels b and c show the schematic and the SEM images of such a solar cell. The PV properties of the solar cells were investigated under a Newport solar simulator with 1 sun AM 1.5G illumination. Figure 5d shows the output characteristics of a typical solar cell with the SiGe wire length of ~3 μm. The dark current−voltage (*I*−*V*) curve of the device shows *I*−*V* characteristics as shown in Figure 5d as well. Under illumination, the device exhibits an open circuit voltage (V_{oc}) of 650 mV, a short current density (J_{sc}) of 8.38 mA/cm^2, and a fill factor of 0.60, giving an energy conversion efficiency (η) of 3.26%. The energy conversion efficiency is obviously higher than that of those multicrystal core/shell structure solar cells, which is around 1%.[42,47] However, there is still a gap between reported experimental efficiencies and the estimated 17% theoretical efficiency.[48,49] We believe the efficiency of such solar cells could be further improved by optimizing the geometries of the wire arrays and the thicknesses and deposition conditions of the thin film layers, by passivating the bottom surface, by decreasing the series resistance, and by increasing the coverage density of the wires. Because of the lithography instrument limitation, the density of the wires is very low and the ratio between the wire and the Si wafer areas is only 0.20. If this factor is increased, the current density and

the energy conversion efficiency could potentially be several times higher.

CONCLUSIONS

In summary, using lithography combined with catalytic etching, large-area (5 in. wafer) arrays of vertical aligned single-crystal Si wires have been prepared with high throughput. This method allows precise control over the diameter, length, density, spacing, orientation, shape, pattern, and location of the Si wires. Obvious and strong evidence is shown to support the catalytic etching mechanism in which the catalyst particles catalyze the etching of Si in contact with them and do not prevent the Si from being etching. In addition, single-crystal epitaxial radial n-Si/p-SiGe junction structures are fabricated by coating single-crystal SiGe layers on the Si wire arrays. Inspired by the excellent antireflection property and unique single crystal epitaxial p-n radial junctions of the SiGe wire arrays, we build solar cells based on the Si/SiGe wire arrays, of which a typical device exhibits V_{oc} of 650 mV, J_{sc} of 8.38 mA/cm^2, and a fill factor of 0.60, giving an energy conversion efficiency (η) of 3.26%. Such a single-crystal epitaxial p−n radial structure will have a great potential application for PV solar energy conversion.

EXPERIMENTAL METHODS

Fabrication of Si Wire Array. Five inch 100-oriented silicon wafers (p-type, resistivity of *ca.* 0.01 ohm cm) were used in the experiments. A layer of photoresist dots was obtained with a standard lithography over a whole Si wafer. Subsequently, a gold film with the thickness of ~15 nm was thermally evaporated on the substrate, at a pressure of 10^{-6} Pa. Then the substrate was immersed in acetone for 2 h to remove the photoresist dots.

For the solution etching process, an etching mixture consisting of deionized water, HF, and H_2O_2 was used at room temperature. The concentrations of HF and H_2O_2 were 4.6 and 0.44 M, respectively. The etching duration varied from 2 to 45 min, depending on the required length of the wires. After etching, the gold film was removed by immersion the arrays in boiling aqua regia (3:1 (v/v) HCl/HNO_3) for 15 min.

UHVCVD Epitaxial Growth. As-prepared Si wires were treated by reactive ion etching (RIE, O_2 pressure 5 Pa, 40SCCM, 50 W, duration 120 s) to reduce the size of the wires and to clean their surface. After that, the Si wafer with the Si wires was thermally oxidized at 1000 °C for 2−4 h, and a 50−100 nm SiO_2 layer was obtained at the surface of the Si wires. After the surface oxide layer was removed by dipping the Si wafer in aqueous HF solution, the surface of the Si wires became fresh, metal-free, and hydrophobic. Then the Si wafer was placed in a UHVCVD instrument (Applied Materials, Inc.) for the epitaxial growth of a p-$Si_{1-x}Ge_x$ (x = 0 and 0.17) layer with *in situ* doping. The base pressure of the UHVCVD chamber was 5×10^{-9} Torr. SiH_4, GeH_4, and B_2H_6 were used as vapor sources. The p-SiGe epitaxial layer was grown at 550 °C for 2 h.

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