

# Direct Heteroepitaxy of Vertical InAs Nanowires on Si Substrates for Broad Band Photovoltaics and Photodetection

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## ABSTRACT

Catalyst-free, direct heteroepitaxial growth of vertical InAs nanowires on Si(111) substrates was accomplished over a large area by metal–organic chemical vapor deposition. Nanowires showed very uniform diameters and a zinc blende crystal structure. The heterojunctions formed at the interface between the n-type InAs nanowires and the p-type Si substrate were exploited to fabricate vertical array photodiode devices which showed an excellent rectification ratio and low reverse leakage current. Temperature-dependent current transport across the heterojunctions was studied theoretically and experimentally in the dark and under AM 1.5 illumination. When operated in photovoltaic mode, the open-circuit voltage was found to increase linearly with decreasing temperature while the energy conversion efficiency changed nonmonotonically with a maximum of 2.5% at 110 K. Modeling of the nanowire/substrate heterojunctions showed good agreement with the experimental observations, and allowed determining the conduction band offset between the InAs nanowires and Si to be 0.10–0.15 eV. The external quantum efficiency and photoresponsivity profiles of the device showed a broad spectral response from the visible to the infrared region, indicating potential applications as a broad band photovoltaic cell or a visible–infrared dual-band photodetector.

Semiconductor nanowires have been successfully utilized as building blocks for various electronic and photonic devices, including field-effect transistors,<sup>1–3</sup> nanolasers,<sup>4–6</sup> light-emitting diodes,<sup>7–9</sup> and energy harvesting devices.<sup>10–23</sup> Vertically aligned semiconductor nanowire arrays are of particular interest for optoelectronic devices such as photovoltaic cells and photodetectors,<sup>12,18,19,21–25</sup> due to their potential to high efficiency and high sensitivity because of the enhanced light absorption,<sup>14</sup> improved carrier collection efficiency,<sup>13,17,26</sup> reduced optical reflectance,<sup>18,23</sup> and longer diffusion length and lifetime for minority carriers compared to conventional thin film devices.<sup>16,27,28</sup> One possible photodiode configuration is the radial homojunction or heterojunction made of core–shell nanowire structure, in which a doped nanowire core is surrounded by a shell with comple-

mentary doping.<sup>12,19,20</sup> This geometry allows achieving high optical absorption due to the long optical path in the axial direction of the vertical nanowires, while reducing considerably the distance over which carriers must diffuse before being collected in the radial direction. Coaxial structures have been reported for optoelectronic devices based on silicon<sup>19–21</sup> and III–V compound semiconductor nanowires.<sup>12</sup> One limitation of core–shell homojunction structures, however, is that they can respond only to a limited portion of the spectrum determined by the semiconductor band gap; core–shell multijunction heterostructures would allow overcoming this limitation but call for a complicated process for synthesis and device fabrication. Moreover, coaxial nanowire structures often suffer from large leakage current and low breakdown voltage due to the small diameter of nanowires and the consequent low tunneling threshold.<sup>12</sup> An alternative photodiode configuration, where heterojunctions are formed by direct integration of vertically aligned nanowire arrays on their growth substrates, particularly on Si substrate, may be promising for photovoltaics and photodetection.<sup>18,24</sup> Although heteroepitaxial growth of high-quality III–V semiconductor films on Si substrates remains challenging due to their large lattice mismatch,<sup>29</sup> lattice matching require-

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ments for nanowire growth are relaxed due to strain accommodation at the nanowire surface,<sup>30–32</sup> and direct heteroepitaxial growth of high quality III–V nanowires on Si substrates has already been achieved.<sup>33–37</sup> Tuning the alloy composition of III–V compound nanowires allows engineering the band diagram of the heterojunctions and consequently makes broad band photovoltaic cells and photodectors possible, opening up opportunities for direct integration of broad band photodectors into CMOS technology. Moreover, the high-quality heteroepitaxy of III–V nanowires on Si substrates enables the experimental study of fundamental properties (such as band structure and carrier transport) of III–V nanowires/Si heterojunctions otherwise not readily available.

The integration of high-quality InAs with Si is of great interest for optoelectronic devices such as infrared photodetectors. The conventional growth of single crystal InAs thin film on Si usually requires ultrahigh vacuum environment and intermediate (buffer) layers to reduce effects from the large lattice mismatch and thermal expansion coefficient.<sup>38–42</sup> In this paper, a simple catalyst-free, vertical epitaxial growth of single crystal InAs nanowires on Si(111) substrate is presented. Nanowire growth was obtained by metal–organic chemical vapor deposition (MOCVD) over a large substrate area and without the use of any predeposited material or mask. Heterojunction photodiode devices based on heteroepitaxial n-type InAs nanowires on p-type Si substrate were demonstrated. The temperature dependence of charge transport across the n-InAs nanowires/p-Si heterojunction photovoltaic cells under illumination was investigated, which allows direct determination of the band discontinuity of the n-InAs nanowires/p-Si heterojunction. The spectral dependence of external quantum efficiency (EQE) and photoresponsivity from the visible to the infrared was also tested.

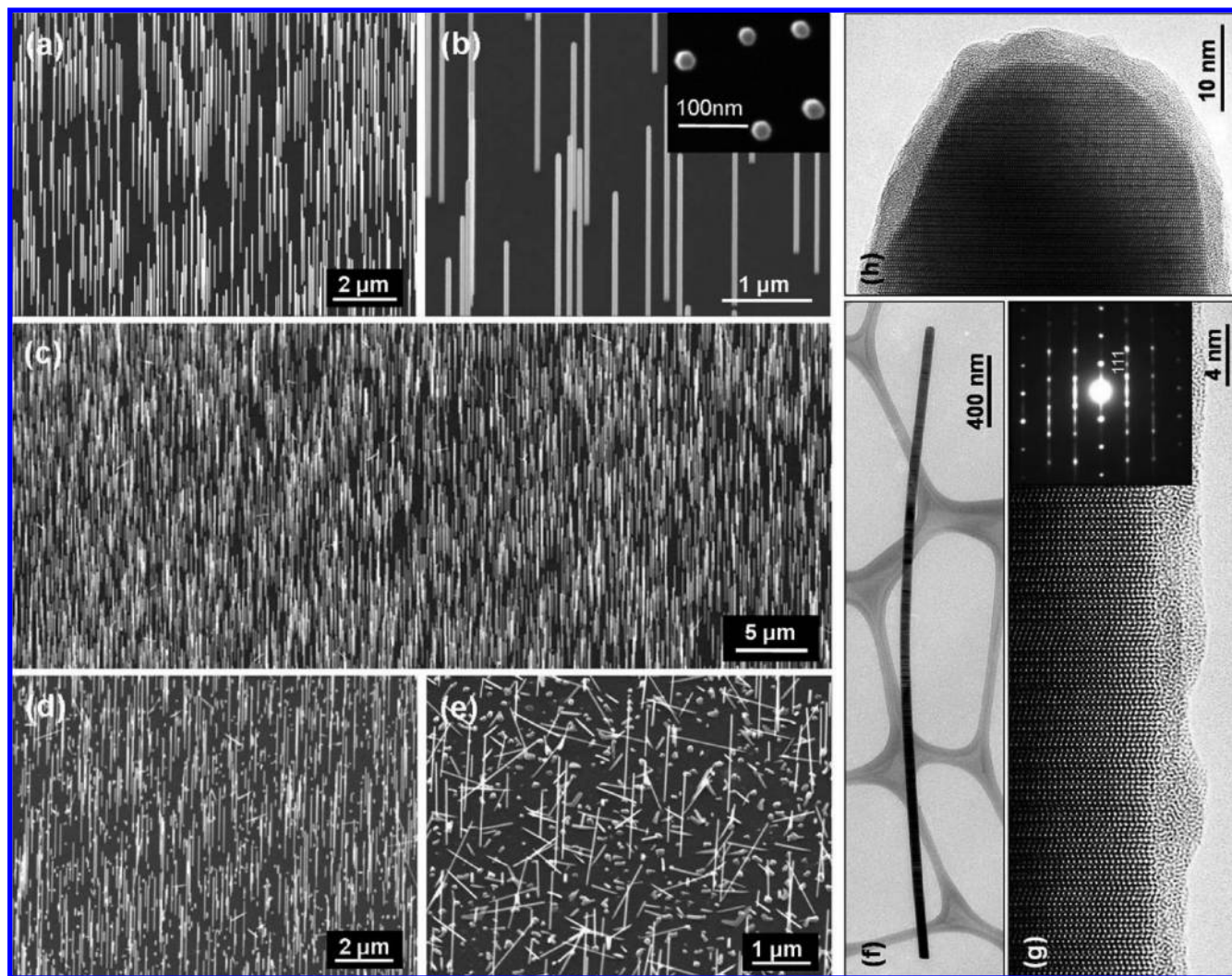
Vertical InAs nanowire arrays were grown in a close-coupled showerhead MOCVD system (Thomas Swan Scientific Equipment, Ltd.). Prime quality p-type Si(111) wafers (MEMC Electronic Material Inc.) were diced and cleaned with solvents in an ultrasonic bath. The substrates were etched using diluted buffered oxide etch (BOE 6:1, Sigma-Aldrich) for 30 s to remove the native oxide, and then rinsed in deionized water for about 15 s and dried with N<sub>2</sub>. The substrates were then loaded into the MOCVD chamber, where growth was performed using arsine (AsH<sub>3</sub>) and trimethylindium (TMI, Akzo Nobel) precursors in H<sub>2</sub> carrier gas (total flow rate of 20 L/min) at 100 Torr chamber pressure. The substrates were heated up to the growth temperature ranging from 535 to 550 °C, and after a short stabilization time, the growth was initiated by simultaneous introduction of AsH<sub>3</sub> and TMI to the reactor chamber with molar fractions of  $2 \times 10^{-4}$  and  $2 \times 10^{-6}$ , respectively. The growth was terminated by interrupting the TMI flow, while the AsH<sub>3</sub> flow was retained until the reactor was cooled down to 250 °C to prevent decomposition of the InAs nanowires.

The morphologies of InAs nanowires were characterized by field-emission scanning electron microscopy (FE-SEM, Phillips XL30). Figure 1a shows the InAs nanowires grown

on a Si substrate that was loaded into the MOCVD chamber immediately after the etching process. An SEM image of large area vertical InAs nanowires with very few islands and nonvertical nanowires is shown in Figure 1c. The higher magnification SEM image (Figure 1b) shows that the nanowires are straight and uniform in diameter with hexagonal cross section (inset of Figure 1b). No large base islands were found at the area surrounding the nanowire root, which is clearly different from that typically found at the base of nanowires grown with Au catalysts,<sup>43</sup> suggesting a different growth mechanism from the Au-catalyzed growth. The nanowire diameters are distributed from 30 to 80 nm with a majority at about 40 nm. No obvious difference on the vertical nanowire growth was observed within the growth temperature from 535 to 550 °C. To understand the nucleation mechanism, growth was conducted on Si substrates when, after etching, the native oxide was allowed to regrow by exposure to humid air (~85% relative humidity at room temperature) for different time. The island formation and the nonvertical nanowire growth increased with reoxidation time of the substrates, becoming noticeable after 24 h (Figure 1d) and dominating after 130 h (Figure 1e) of native oxide reformation. It is noteworthy that no nanowire growth was observed on the Si substrates without etching the native oxide under the identical growth conditions.

Figure 1f shows the transmission electron microscopy (TEM) image of an InAs nanowire. The nanowire is very uniform in diameter. No metal droplet was observed on the nanowire tip, which is different from that observed in the case of self-catalyzed growth of GaAs nanowires.<sup>44</sup> The uniformity of nanowires and the absence of the catalyst particles on the tips suggest a catalyst-free growth mechanism, since the diminishment and eventual disappearance of the catalysts will result in tapered nanowires with sharp tips.<sup>45</sup> Besides simplifying the fabrication process, catalyst-free nanowire synthesis should also benefit device performance since Au, a catalyst most commonly used for nanowire growth, is known to incorporate into nanowires during growth<sup>46</sup> and cause deep level traps in semiconductors.<sup>47</sup> The electron diffraction pattern (inset of Figure 1g) shows that the nanowire has a zinc blende single crystal structure and grows along the  $\langle 111 \rangle$  direction normal to the Si(111) substrate. High-density twins and stacking faults were found over the entire nanowire length, as well as on the nanowire tip (Figure 1, panels g and h).

The morphology and crystal structure of the InAs nanowires reported here are very similar to those observed in the growth using the organic coating<sup>35</sup> and the selective area patterning<sup>36</sup> methods, where it is understood that after nucleation nanowires elongate preferentially along the  $\langle 111 \rangle$  direction while the lateral growth on the  $\{110\}$  sidewall facets is inhibited under certain growth conditions. A significant difference from the reported organic coating and the selective area methods is that no template or mask is used to assist the nanowire growth. However, the nanowire nucleation mechanism is not entirely clear at this point. One possibility is that the nanowires are mediated by the self-assembled InAs islands on atomic flat Si substrate. After



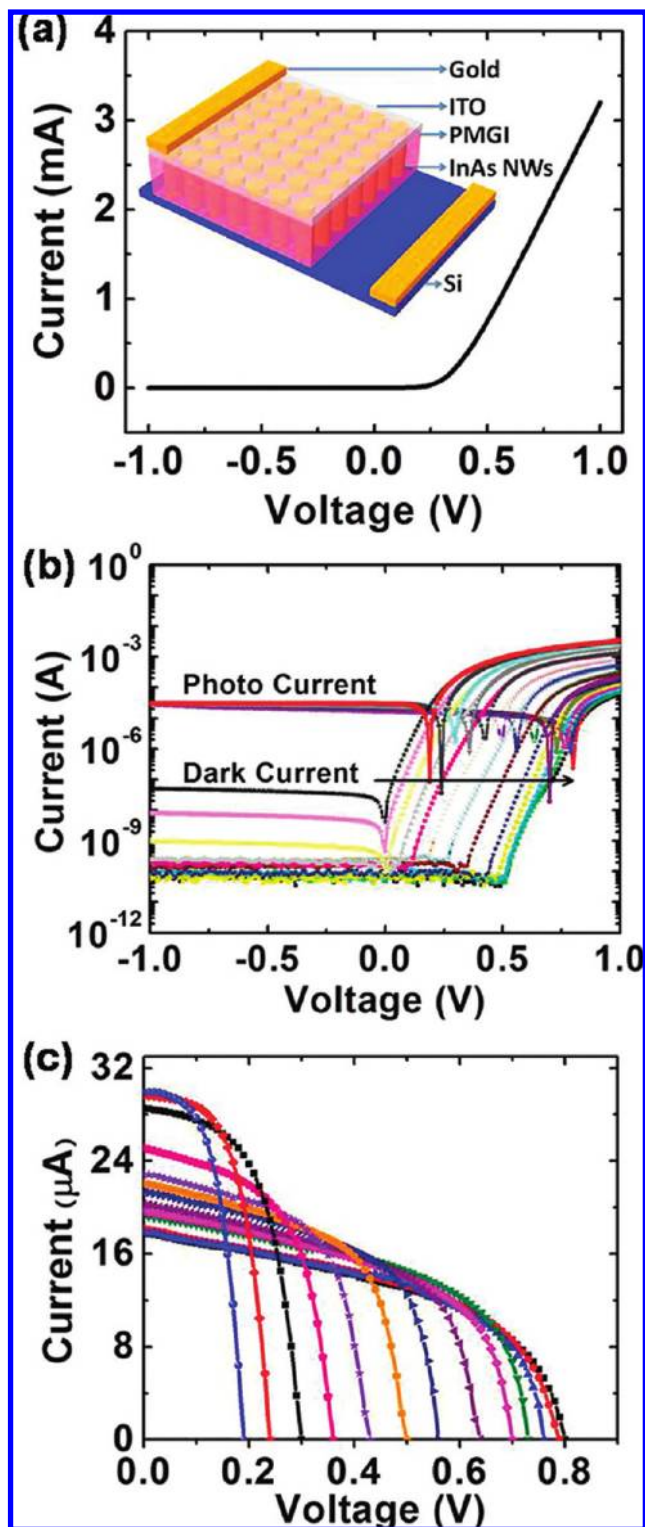
**Figure 1.** FE-SEM (45° tilted view) and TEM images of the InAs nanowires grown for 5 min on Si(111) substrates (a) immediately after the etching (grown at 550 °C), (d) reoxidized for 24 h (grown at 550 °C), and (e) reoxidized for 130 h (grown at 535 °C). (b) Higher magnification SEM image of the nanowires in (a). The inset is a top view image. (c) SEM image of vertical InAs nanowires over a large area. (f) Low-resolution TEM image of the nanowire. (g) High-resolution image of a portion of the nanowire; the corresponding electron diffraction pattern is shown in the inset. (h) High-resolution image of the nanowire tip.

BOE etching, the Si surface is atomically flat and the hydrogen termination makes it relatively stable within a few minutes.<sup>48,49</sup> Due to the large lattice mismatch between InAs and Si, self-assembled InAs islands (nuclei) grow on the oxide-free Si surface with the Volmer–Weber island growth mode<sup>50</sup> under certain growth conditions. In plane InAs thin film growth is not energetically favorable because of the high interfacial surface energy caused by the lattice strain. In the mean time, nanowire growth along one axial direction is preferred since the strain energy can be relieved via lateral relaxation.<sup>30–32</sup> These InAs islands mediate the nanowire growth, and only the islands with sizes smaller than the critical diameter<sup>30–32</sup> can develop epitaxial nanowires in vertical directions. The islands larger than the critical diameter cannot maintain the high-quality heteroepitaxy and the defects and dislocations will initiate nanowire growth along other directions. Benefited from the atomically flat surface, the epitaxial growth occurs mostly along the vertical  $\langle 111 \rangle$  direction rather than other equivalent  $\langle 111 \rangle$  directions.

Upon surface reoxidation, thin oxide ( $\text{SiO}_x$ ) islands provide competing nucleation sites and reactant sinks<sup>50</sup> which could assist and increase the growth of large InAs islands and nonvertical nanowires, as shown in panels d and e of Figure 1. For unetched (with native oxide) or completely reoxidized Si substrates, the Si surface is not exposed and the InAs islands cannot directly nucleate on the oxide; thus no nanowire growth was observed.

From back-gated field-effect transistor (FET) tests (see Figure S1 in Supporting Information, ), the as-grown InAs nanowires show a typical n-type behavior with average electron mobility and concentration around  $1000 \text{ cm}^2/(\text{V s})$  and  $10^{18}–10^{19} \text{ cm}^{-3}$  at room temperature, respectively, which indicates that the InAs nanowires are mildly degenerate, and the Fermi level is almost pinned to the conduction band.<sup>51</sup> A two-terminal heterojunction photodiode was fabricated from the as-grown samples of epitaxial n-type InAs nanowires on the p-type Si substrate, as illustrated in the inset of Figure 2. InAs nanowires were embedded in 600 nm thick

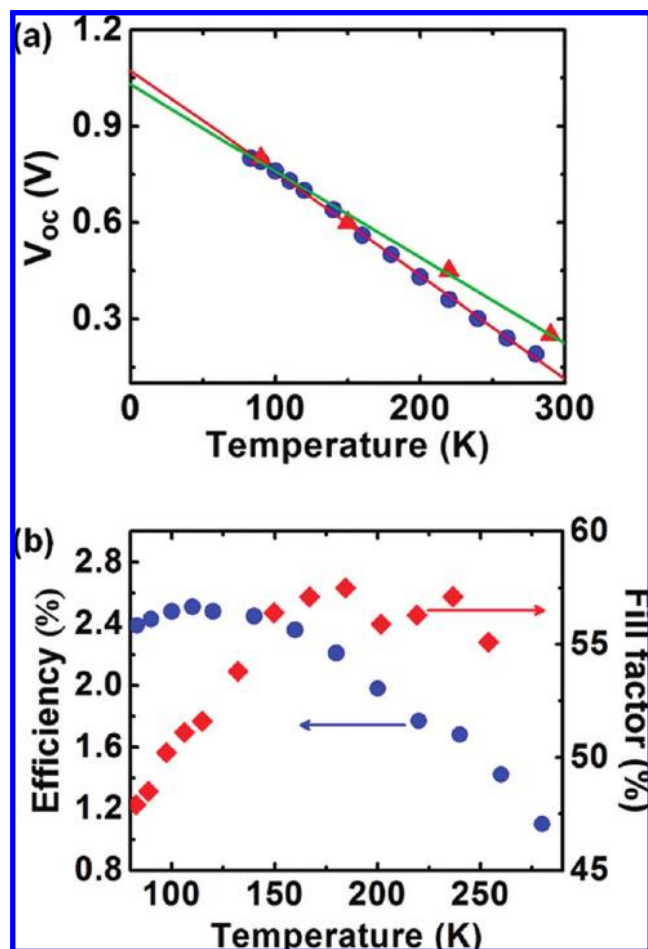




**Figure 2.** (a)  $I$ – $V$  characteristic of the heterojunction in dark at room temperature. The inset is a schematic illustration of the device configuration. (b) Temperature-dependent  $I$ – $V$  characteristics of the heterojunction in dark and under AM 1.5 spectrum illumination with intensity of  $2.86 \text{ mW/cm}^2$ . The arrow indicates the temperature decrease from 280 K, through 260, 240, 220, 200, 180, 160, 140, 120, 110, 100, 90, and finally to 83 K. The absolute value of the current has been plotted on a semilogarithmic scale. The current cutoff at around  $10^{-10} \text{ A}$  is due to the sensitivity of the testing system. (c) Linear plot of the photovoltaic characteristics shown in (b). The leftmost curve (blue circles) corresponds to  $T = 280 \text{ K}$ , while the rightmost curve (black squares) corresponds to  $T = 83 \text{ K}$ .

poly(methylglutarimide) (PMGI, Microchem) insulating layer, and 110 nm thick indium tin oxide (ITO) was deposited as a top contact to the InAs nanowires. Gold electrodes were deposited at the edge of the top ITO pad and on the bottom Si substrate to ensure a good electrical contact. PMGI and ITO are nearly transparent to visible and near-infrared light,<sup>52</sup> allowing a significant amount of the optical excitation to reach the junction region at the nanowires/substrate interface. Current–voltage ( $I$ – $V$ ) characteristics were tested at various temperatures in a liquid nitrogen cryostat by a current–voltage sourcemeter (Keithley 2410). A rectification ratio greater than  $10^4$  at  $\pm 0.5 \text{ V}$  bias and low reverse leakage current ( $\sim 10^{-8} \text{ A}$ ) were achieved at room temperature, implying high-quality p–n junctions formed between the n-type InAs nanowires and p-type Si substrate. A diode ideality factor about 1.5 was extracted from the  $I$ – $V$  data shown in Figure 2a.

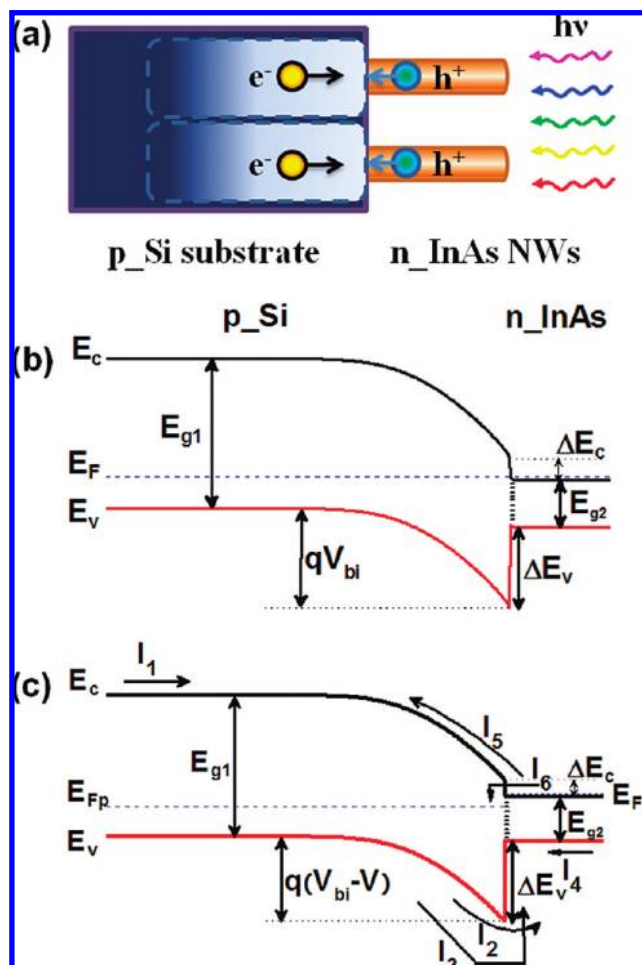
To further understand the current transport properties of this heterojunction, temperature-dependent  $I$ – $V$  curves were measured in the dark and under illumination with air mass 1.5 (AM 1.5) spectrum, as shown in Figure 2b (data presented in semilogarithmic scale) and Figure 2c (data presented in linear scale). At room temperature, the photocurrent at reverse bias is nearly  $10^3$  times larger than the dark current, even at a relatively small incident power intensity of  $2.86 \text{ mW/cm}^2$  (Figure 2b), indicating a very strong photoresponse to white light. The saturated photocurrent at reverse bias is temperature independent while, at forward bias, the series resistance leads to an almost linear photocurrent increase with voltage in the higher voltage region. Unlike conventional p–n junctions,<sup>15,53</sup> however, in this case the dark current at forward bias shows only one linear portion, instead of two, when plotted in semilogarithmic scale (Figure 2b), presumably due to the dominating hole current transport of the heterojunction. The  $V_{oc}$  in Figure 2b increases when temperature is reduced, and at the same time the short circuit current ( $I_{sc}$ ) decreases due to the reduction of thermally generated carriers. The  $V_{oc}$  decreases linearly with increasing temperature (Figure 3a), a behavior that is expected for p–n homojunction photodiodes and that has also been previously reported for heterojunction photodiodes.<sup>54</sup> The slope of  $V_{oc}$  vs temperature and intercept with the ordinate axis  $V_{oc}$  (at  $T = 0 \text{ K}$ ) in Figure 3a are directly related to the incident light intensity and the band diagram of the heterojunction, respectively, which is going to be discussed in detail later. Figure 3b presents the energy conversion efficiency (ECE) and fill factor (FF) of the device at different temperatures, which are calculated as  $ECE = (I_{max} V_{max} FF) / P_{in}$  and  $FF = (I_{max} V_{max}) / (I_{sc} V_{oc})$ , where  $I_{max}$  and  $V_{max}$  are the current and voltage at maximum power points of the  $I$ – $V$  curves shown in Figure 2c, and  $P_{in}$  is the incident power intensity. Independent measurements of the photovoltaic heterojunction at room temperature and under standard AM 1.5 conditions ( $I = 100 \text{ mW/cm}^2$ ) have yielded  $ECE \sim 0.76\%$ , which is consistent with  $ECE \sim 0.73\%$  obtained at room temperature but at a lower illumination intensity ( $2.86 \text{ mW/cm}^2$ ) inside the cryostat. Interestingly, when the temperature is reduced, the ECE increases at first, reaches a maximum of 2.5% at around  $T = 110 \text{ K}$ , and then



**Figure 3.** (a)  $V_{oc}$  versus temperature for two independent devices tested under different incident light intensity. The blue circles are data extracted from Figure 2 under the intensity of  $2.86 \text{ mW/cm}^2$ . The red triangles are data tested under a higher intensity. Both sets of measurements showed linear dependence of  $V_{oc}$  on temperature. (b) Energy conversion efficiency (blue dots) and fill factor (red diamonds) extracted from the data in Figure 2 at different temperatures. The actual area of the device is  $0.1 \text{ cm}^2$

slightly drops down by further lowering the temperature (blue dots in Figure 3b). The initial increase of the efficiency correlates with the increase of  $V_{oc}$  with decreasing temperature, while its decrease at low temperature may be attributed to the poorer FF (red diamonds in Figure 3b) caused by an increase in series resistance<sup>55</sup> (see also Supporting Information). The ECE of the photodiode can be improved by increasing the physical fill factor of the InAs nanowires and decreasing the series resistance. Additionally, the photosensitivity to infrared light could be further enhanced by using more infrared-transparent electrodes, such as carbon nanotube networks,<sup>56</sup> instead of ITO.

The physics underlying charge carrier photogeneration and transport in the n-InAs nanowire/p-Si device can be better understood by considering the built-in electric field and the energy band diagram at the heterojunction interface (Figure 4). Figure 4a schematically presents the separation of photogenerated minority carriers from majority carriers by a built-in electric field in the depletion region. The built-in potential in n-InAs nanowires side of the junction can be



**Figure 4.** (a) Schematic illustration of the separation of photogenerated minority carriers from majority carriers by the built-in electric field across the heterojunction. (b) Band diagram of the nanowire/substrate heterojunction at thermal equilibrium in dark and (c) under illumination at forward bias.  $I_1$  to  $I_6$  indicate the current components across the heterojunction under illumination: electron photocurrent ( $I_1$ ), hole emission current ( $I_2$ ), hole current due to recombination at the interface traps ( $I_3$ ), hole photocurrent ( $I_4$ ), electron diffusion current ( $I_5$ ), and electron current due to recombination at the interface traps ( $I_6$ ). For simplicity, tunneling current through the heterojunction at low voltage is not considered. Notice that the arrows indicate the actual directions of carrier flow.

neglected, and the voltage drops entirely in the Si side of the junction under an applied bias.<sup>57</sup> Parts b and c of Figure 4 schematically show the energy band diagram for the heterojunction at thermal equilibrium in dark and under illumination at forward bias, respectively. Note that, in this nanowire/Si heterojunction, the active junction area is given by the sum of all the nanowire cross-sectional areas, which is much smaller than the depletion region cross-sectional area in p-Si. It is known that the  $V_{oc}$  of a photodiode is limited by the built-in potential of the junction ( $V_{bi}$ ).<sup>58</sup> For our n-InAs/p-Si heterojunction photodiode,  $V_{oc}$  reached  $0.8 \text{ V}$  at  $83 \text{ K}$  indicating a large built-in potential, therefore a relatively large valence band offset,  $\Delta E_v$  ( $E_{g2} + \Delta E_v > qV_{bi}$ ), and a small conduction band offset,  $\Delta E_c$  ( $E_{g1} - \Delta E_c > qV_{bi}$ ). Note that in the nanowire case, the presence of surface states, strain, and possibly stacking faults near the junction may

considerably change the band discontinuity compared to the bulk case.

As shown in Figure 4c, six current components are possibly generated across the heterojunction under forward bias, due to electron photocurrent ( $I_1$ ), hole emission current ( $I_2$ ), hole current due to interface recombination ( $I_3$ ), hole photocurrent ( $I_4$ ), electron diffusion current ( $I_5$ ), and electron current due to interface recombination ( $I_6$ ). The overall current of the device under illumination can be obtained by analyzing the six currents and calculating the net current across the junction. Among the current components,  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_6$  are the most relevant. Under white light illumination,  $I_4$  is relatively small due to the large valence band offset, smaller depletion region, and minority carrier diffusion length in heavily doped InAs nanowire compared with p-Si.  $I_5$  is negligible compared to  $I_2$  because the electron diffusion velocity is much smaller than the hole thermionic emission velocity in p-Si.<sup>59</sup> The magnitude of the recombination current is dominated by the number of holes that reach the heterointerface via valence band in Si as well as the density of interface states.<sup>60</sup> Due to the nature of recombination, hole current  $I_3$  must equal to the electron current  $I_6$  here. Therefore the total current across the heterojunction can be assumed to be

$$I = I_{\text{dark}} - I_{\text{ph}} \approx (I_2 + I_3) - (I_1 + I_4) \quad (1)$$

where  $I_2 + I_3$  represent the dark current ( $I_{\text{dark}}$ ) and  $(I_1 + I_4)$  the photocurrent ( $I_{\text{ph}}$ ). The photocurrent  $I_{\text{ph}}$  is given by

$$I_{\text{ph}} = I_1 + I_4 = qG_1(A_1 - A_2)(X_1 + L_{n1}) + qG_2A_2(X_2 + L_{p2}) \quad (2)$$

where  $q$  is the elementary charge,  $G_1$ ,  $X_1$ ,  $L_{n1}$ , and  $G_2$ ,  $X_2$ ,  $L_{p2}$  are the net photogeneration–recombination rate per unit volume, length of depletion region, and minority carrier diffusion length in p-Si and in n-InAs nanowires, respectively.  $A_1$  is the sum of all the cross-sectional areas of the depletion cylinders in Si,<sup>59</sup> while  $A_2$  is the sum of all the nanowire cross-section areas (the active junction area of the device). Because the Fermi level is very close to the conduction band edge of InAs (see Figure 4b), we have  $E_F - E_{v1} + qV_{\text{bi}} \approx E_{g2} + \Delta E_v = E_{g1} - \Delta E_c$ , where  $E_F - E_{v1}$ , if not specifically coordinated, indicates the difference between the Fermi level and the valence band edge in p-Si bulk region beyond the depletion region at equilibrium. Because of the large potential barrier in the valence band shown in Figure 4c, the conduction mechanism for hole current  $I_2$  is governed by thermionic emission of holes in p-Si. The current density is therefore given by<sup>61</sup>

$$I_2 = qp_{10}A_2\sqrt{\frac{kT}{2\pi m_1^*}} \exp\left(-\frac{qV_{\text{bi}}}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] = qA_2\sqrt{\frac{kT}{2\pi m_1^*}} N_{v1} \exp\left(-\frac{E_{g1} - \Delta E_c}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (3)$$

here  $N_{v1}$  is the effective density of states in valence band of

p-Si,  $p_{10} = N_{v1} \exp[(E_{v1} - E_F)/kT]$  is the hole concentration in bulk p-Si region beyond the depletion region at equilibrium,  $m_1^*$  is the effective mass of holes,  $k$  is the Boltzmann's constant, and  $V$  is the applied voltage. The interface recombination current  $I_3$  is given by the relation<sup>60,62,63</sup>

$$I_3 = qA_2S_{\text{int}}N_{v1} \exp\left[-\frac{E_{g1} - \Delta E_c}{kT}\right] \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (4)$$

in which  $S_{\text{int}}$  is the recombination velocity at the interface, a factor that involves the density of interface states and capture cross section,<sup>53</sup> and is expected to be relatively small in our device due to the high-quality abrupt nanowire/substrate heterojunctions which are nearly free from interface states.

Substituting eqs 2, 3, and 4 into eq 1 yields the following current–voltage relationship

$$I = qA_2N_{v1} \left[ \left(\frac{kT}{2\pi m_1^*}\right)^{1/2} + S_{\text{int}} \right] \exp\left(-\frac{E_{g1} - \Delta E_c}{kT}\right) \left[ \exp\left(\frac{qV}{kT}\right) - 1 \right] - I_{\text{ph}} \quad (5)$$

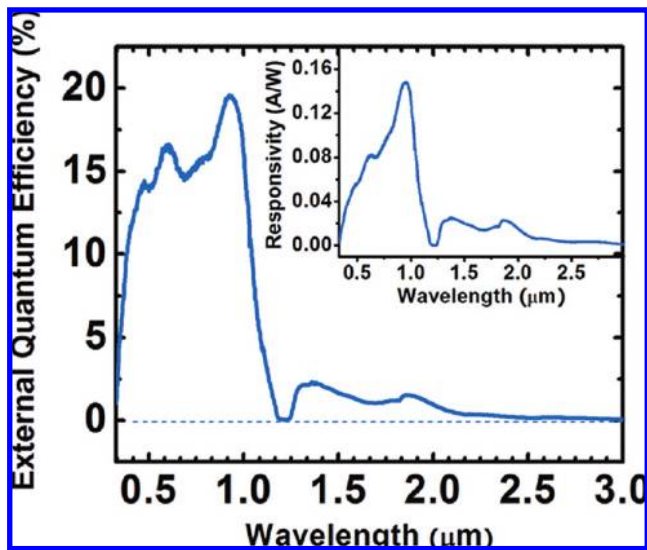
Note that the carrier recombination at nanowire sidewalls is not considered in eq 5 for simplicity. Our previous study has shown that the surface states, along with the internal electric field from nanowire center to the surface, facilitate charge separation and trapping of one type of charges, which actually enhances the carrier lifetime.<sup>25</sup> By consideration of the series resistance and the ideality factor, the  $I$ – $V$  relationship of the InAs nanowires/Si heterojunction falls into a similar form proposed by Boer and Rothwarf for conventional thin film photovoltaic cells,<sup>64</sup> in which the  $I$ – $V$  characteristic is explained as a diode characteristic shifted by the photo-generated current  $I = I_0\{\exp[q(V - IR_s)/\gamma kT] - 1\} - I_{\text{ph}}$  where  $R_s$  is the series resistance of the system,  $\gamma$  the ideality factor of the diode, and  $I_0 = qA_2N_{v1}[(kT/2\pi m_1^*)^{1/2} + S_{\text{int}}] \exp[-(E_{g1} - \Delta E_c)/kT] = I_{00} \exp[-(E_{g1} - \Delta E_c)/kT]$ . Note that for typical p–n diodes, the dark current plotted versus voltage in semilogarithmic scale typically shows two linear portions: the first, characterized by a smaller slope, appears in the low voltage regime and is predominantly related to carrier recombination, while the second, with relatively larger slope, is related to carrier diffusion.<sup>53</sup> Our model predicts that only one type of carrier (holes) dominates the current transport of the heterojunction in the dark ( $I_5 \ll I_2$ )<sup>59</sup> due to the lack of electrons diffusing into the depletion region and therein recombining with holes. This point is validated by the observation of a single linear portion in our device (Figure. 2b).

The functional dependence of  $V_{\text{oc}}$  on temperature can be obtained by setting eq 5 to be zero

$$qV_{\text{oc}} = E_{g1} - \Delta E_c + kT \ln(I_{\text{ph}}/I_{00}) \quad (6)$$

For simplicity, here we neglect the mild temperature dependence of  $E_{g1}$  and  $\ln(I_{\text{ph}}/I_{00})$ . Thus eq 6 predicts a negative linear dependence of the open-circuit voltage on





**Figure 5.** External quantum efficiency spectrum of the p-Si/n-InAs heterojunction photodiode tested without bias. The inset shows the photoresponsivity profile of the photodiode.

temperature, which is consistent with our experimental results. The value of  $(E_{g1} - \Delta E_c)$  can be estimated by extrapolating  $qV_{oc}$  versus  $T$  to  $T = 0$  K as the intercept with the ordinate axis. Assuming the band gap of Si at  $T = 0$  K as 1.17 eV, the  $\Delta E_c$  of the heterojunction can be estimated to be  $\sim 0.10$ – $0.15$  eV. As previously mentioned, in the case of nanowires, this value is significantly lower than the conduction band offset predicted by the Anderson model for bulk InAs/Si heterojunction ( $\Delta E_c = 0.85$  eV).<sup>61</sup> It is important to note that the conduction band gap offset  $\Delta E_c$  is directly related to fundamental material properties and is assumed to be independent of the light intensity, bias voltage, and the device fabrication process.<sup>62,65</sup> This assumption is consistent with the fact that the two sets of data from different devices tested under different incident light intensity (Figure 3a) have similar intercepts at  $T = 0$  K. Equation 6 also predicts that the slope of  $V_{oc}$  versus  $T$  increases at higher irradiance (for higher  $I_{ph}$ ), as observed experimentally (Figure 3a).

The EQE spectrum and photoresponsivity of the p-Si/n-InAs heterojunction photodiode under zero bias was obtained using the conventional modulation technique, where light emitted by a halogen lamp was dispersed by a monochromator (Horiba Jobin Yvon iHR-550), modulated at a frequency of 134 Hz by a mechanical chopper (EG&G-PAR 197), and focused onto the sample; the photocurrent was measured by a lock-in amplifier (Stanford Research SR520) without bias and was corrected by the spectral intensity of light excitation. The EQE was calculated as

$$EQE_{\lambda} = \frac{R_{\lambda} hc}{\lambda q}$$

where  $R_{\lambda}$  is the photoresponsivity,  $R_{\lambda} = J_{\lambda}/P_{\lambda}$ , with  $\lambda$  the wavelength of the incident light,  $h$  the Planck constant,  $c$  the speed of light in vacuum,  $q$  the elementary charge,  $J_{\lambda}$  the photocurrent, and  $P_{\lambda}$  the incident power intensity at the wavelength of  $\lambda$ . Figure 5 and inset present the EQE spectrum and photoresponsivity of the device, showing

photoresponse to both visible and infrared illumination. Below the Si absorption edge ( $\lambda > 1200$  nm), only the InAs nanowires contribute to the photocurrent ( $I_4$ ), while above the Si absorption edge, both Si and InAs give their contribution ( $I_1$  and  $I_4$ ). The EQE and the photoresponsivity show a minimum at around 1200 nm, corresponding to the absorption edge of silicon. This is not fully understood and might be attributed to the nearly complete depletion of carriers due to recombination when the concentration of carriers photo-generated in Si is comparable to that in InAs nanowires.

Direct integration of multiple band gap absorber materials as in this prototype InAs/Si heterojunction allows harvesting solar energy from the wide solar spectrum which, combined with the enhanced light absorption offered by nanowire arrays, could eventually lead to an increase of energy conversion efficiency of photovoltaic cells. On the other hand, more and more interest has been focused on developing p–n heterojunction photodetectors due to their low-frequency noise, fast response time, and very low power dissipation.<sup>66</sup> The sensitivity to both visible and infrared light could also enable this photodiode to be used as a multispectral photodetector to detect either visible or infrared light and opens up opportunities for integration of III–V photoactive elements to CMOS technology.

To summarize, large area, heteroepitaxial growth of vertical InAs nanowire arrays on Si substrates was accomplished without using any metal catalysts or templates. The InAs nanowires have a zinc blende single crystal structure and grow along the  $\langle 111 \rangle$  direction with no measurable tapering. Heterojunction photodiodes were fabricated by directly integrating vertically aligned n-type InAs nanowires arrays on p-type Si, which showed a rectification ratio greater than  $10^4$  at  $\pm 0.5$  V in dark and low reverse leakage current ( $\sim 10^{-8}$  A) at room temperature. Temperature-dependent current transport of the heterojunction was tested in the dark and under AM 1.5 illumination. The ECE increases with decreasing temperature and reaches the maximum about 2.5% at 110 K. The charge transport across the n-InAs nanowire/p-Si heterojunction under illumination satisfies the generic  $I$ – $V$  relationship for photovoltaic cells proposed by Boer and Rothwarf.<sup>64</sup> The  $V_{oc}$  increases linearly with decreasing temperature according to the theoretical prediction, allowing quantification of the band discontinuity of the heterojunction. EQE and photoresponsivity spectral measurements of the device showed a good response to both visible and infrared illumination, which demonstrates the potential of this kind of structure as wide spectrum photovoltaic cells or visible–infrared dual-band photodetectors. Significantly, this research demonstrates direct and contamination-free integration of InAs nanowires with Si for electronic and photonic applications, a scheme that could also be extended to other III–V materials.

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**Supporting Information Available:** The characterization of the transport properties of single InAs nanowire and the analysis of the temperature-dependent energy conversion efficiency and fill factor. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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- (60) Because the InAs nanowires are mildly degenerate, the electron density in InAs is quite high. The interface recombination current for p-Si/n-InAs heterojunction is therefore dominated by the number of holes that reach the interface via valence band in Si as well as the density of interface states to serve as the recombination centers. The interface recombination current is given by  $I_3 = qS_{int}A_2N_{v1} \exp\{-[E_F(x=0) -$



$E_{\nu 1}(x=0)/kT\}[\exp(qV/kT)-1]$ , where  $x = 0$  indicates the coordinate of the interface.  $S_{\text{int}}$  is the recombination velocity at the interface, a factor that is determined by the density of interface states and capture cross section. Because the Fermi level is very close to the conduction band edge of InAs (see Figure 4b), we can substitute  $E_{\text{F}}(x=0) - E_{\nu 1}(x=0)$  for  $E_{\text{g}1} - \Delta E_{\text{c}}$  to get eq 4.

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