

High-performance pentacene field-effect transistors using Al₂O₃ gate dielectrics prepared by atomic layer deposition (ALD)

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Abstract

High-performance pentacene field-effect transistors have been fabricated using Al₂O₃ as a gate dielectric material grown by atomic layer deposition (ALD). Hole mobility values of $1.5 \pm 0.2 \text{ cm}^2/\text{V s}$ and $0.9 \pm 0.1 \text{ cm}^2/\text{V s}$ were obtained when using heavily *n*-doped silicon (*n*⁺-Si) and ITO-coated glass as gate electrodes, respectively. These transistors were operated in enhancement mode with a zero turn-on voltage and exhibited a low threshold voltage ($< -10 \text{ V}$) as well as a low sub-threshold slope ($< 1 \text{ V/decade}$) and an on/off current ratio larger than 10^6 . Atomic force microscopy (AFM) images of pentacene films on Al₂O₃ treated with octadecyltrichlorosilane (OTS) revealed well-ordered island formation, and X-ray diffraction patterns showed characteristics of a “thin film” phase. Low surface trap density and high capacitance density of Al₂O₃ gate insulators also contributed to the high performance of pentacene field-effect transistors.

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Keywords: Organic field-effect transistors (OFETs); Atomic layer deposition (ALD); Al₂O₃; Pentacene; ITO

1. Introduction

Organic field-effect transistors (OFETs) have recently gained attention as building blocks for electronic applications that can greatly benefit from low-cost, large-area fabrication and flexible form factors, such as radio-frequency identification tags

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(RFID) [1], drivers for electronic paper [2] and driving circuits for flat panel displays (FPDs) [3]. To achieve high-performance OFETs, development of suitable gate dielectric materials in addition to high-mobility organic semiconductors is important. Preferably, dielectric materials should have a high dielectric constant (κ) and should be processible into thin high-quality, defect-free films to form OFETs with a reduced operating voltage, fast switching speed, and large on/off ratio. Low deposition temperature is also desirable to allow for fabrication on plastic substrates. Atomic layer deposition (ALD) is a deposition technique that allows for the deposition of highly conformal, defect-free dielectric layers at relatively low temperature [4–7]. Dielectric films grown by ALD have a high resistivity and good barrier properties, and therefore are excellent candidates for gate insulators. The deposition process is simple, low-cost, and compatible with various substrates made from different materials and with irregular shapes [4,5]. Oxide layers fabricated by ALD have also been studied as O_2/H_2O barriers for organic light-emitting diodes [8]. However, to date ALD technology has had limited success in fabricating dielectric materials suitable for OFET applications [9,10].

Here, we report on the fabrication of high-performance pentacene OFET devices using a 200 nm-thick film of Al_2O_3 grown by ALD as the gate dielectric material. We first characterized the dielectric and the surface properties of Al_2O_3 thin films grown by ALD. We then fabricated OFETs on heavily n -doped silicon (n^+ -Si) substrates (serving also as the gate electrode) with both, 200 nm-thick films of Al_2O_3 grown by ALD and thermally-grown SiO_2 , as the gate dielectrics. The latter was used as a reference control sample. Finally, we used the conformational aspect of ALD to fabricate high-performance OFETs on a substrate with a large surface roughness: ITO-coated glass substrate.

2. Deposition and characterization of Al_2O_3 gate insulators

A Savannah100 ALD system from Cambridge Nanotech Inc. was used to deposit Al_2O_3 dielectric films on n^+ -Si substrates ($5 \times 10^{-3} \Omega \text{ cm}$) and on ITO-coated glass substrates (Colorado Concept Coatings, $60 \Omega/\text{sq.}$). ITO-coated glass substrates were cleaned in an ultrasonic bath using, successively, soapy water, deionized water, acetone, and

reagent alcohol for 15 min each, and then dried under nitrogen. The n^+ -Si substrates were cleaned in a mixture of H_2SO_4/H_2O_2 , and a buffered oxide etchant (1:6 diluted HF in H_2O) was used to remove the natural oxide. Immediately before being loaded into the ALD deposition system, substrates underwent O_2 plasma treatment in a plasma asher for 10 min at low power. This plasma treatment is known, not only to remove organic residues and other contaminants from surfaces, but also to increase the concentration of surface hydroxyl groups and the amount of absorbed aluminum precursor [11]. Al_2O_3 films were deposited at 100°C using alternating exposures of $Al(\text{CH}_3)_3$ and H_2O vapor at a deposition rate of approximately 1 \AA per cycle. Each deposition cycle (one monolayer) lasted 24 s, yielding a total deposition time of 13.3 h for 2000 cycles. The thickness of the Al_2O_3 films was measured by a stylus profilometer (Dektak 6M by Veeco) and found to be about 200 nm.

We characterized the dielectric properties of Al_2O_3 films (200 nm) grown on ITO-coated glass using parallel plate capacitors of various plate areas ranging from $3.1 \times 10^{-3} \text{ cm}^2$ to $2.4 \times 10^{-1} \text{ cm}^2$. The capacitors were fabricated by sandwiching a 200 nm-thick Al_2O_3 film between an ITO electrode and a 100 nm-thick Al electrode. For each of the 12 devices, capacitance and dissipation factor (loss tangent) were measured at $1.0 V_{\text{RMS}}$ as a function of frequency from 20 Hz to 1 MHz with an Agilent 4284A precision LCR meter. The dielectric constant (κ) of Al_2O_3 at 1 kHz was determined to be 7.5 ± 0.2 (calculated from the linear dependence of capacitance as a function of device area $C_{\text{OX}} = \epsilon_0 \kappa / t$, where ϵ_0 is the permittivity in vacuum, t is the thickness, and κ is the dielectric constant). This result is comparable to the value obtained by Groner [5]. The current density vs. voltage characteristic presented in Fig. 1a shows that a 200 nm-thick Al_2O_3 film is an excellent insulator with a leakage current density less than 200 nA/cm^2 under an applied field of 2 MV/cm over a contact area of 0.016 cm^2 . Notably, these values are small considering the large surface roughness of ITO-coated glass. Dissipation factors for all devices were measured in the range of 10^{-3} . Furthermore, the capacitance density C_{OX} was stable up to a relatively high frequency of 1 MHz, as shown in Fig. 1b.

In addition to dielectric properties, the chemical and physical surface properties of dielectrics including surface wetting properties, surface roughness, and surface defect density are also important

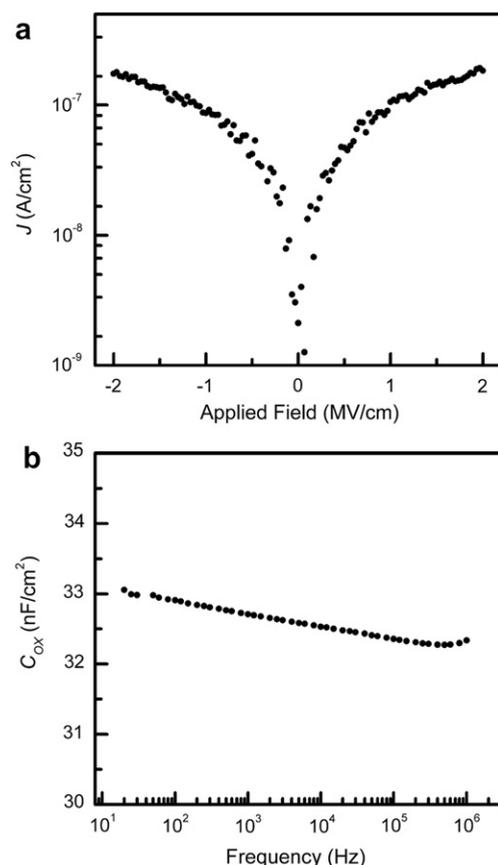


Fig. 1. (a) Current density (J) vs. applied field characteristics and (b) capacitance density (C_{OX}) vs. frequency characteristics of capacitors prepared with ALD-grown Al_2O_3 dielectric materials on ITO-coated glass substrates.

parameters that affect the electrical performance of OFETs, through the morphology/structural ordering of organic semiconductor films and the charge transport at the dielectric/semiconductor interface. To characterize the surface properties, first, an element analysis of Al_2O_3 films was done by energy dispersive spectrometry (EDS). No other elements other than Al, O, and elements from the substrates (e.g., Si, In, and Sn) were detected over a test area of $10\ \mu m \times 10\ \mu m$. Then, the surface morphology of Al_2O_3 on both n^+ -Si substrates (smooth) and on ITO-coated glass (rough) was investigated by AFM (Digital Instruments NanoScope™ Scanning Probe Microscopes). The results were compared with thermally-grown SiO_2 on n^+ -Si substrates as shown in Fig. 2. The root-mean-square (RMS) surface roughness of the 200 nm-thick Al_2O_3 film on an n^+ -Si substrate was estimated to be 4.3 Å when measured over an area of $1\ \mu m \times 1\ \mu m$ (Fig. 2 left), which is almost identical to that of the 200 nm-thick

SiO_2 film thermally-grown on an identical n^+ -Si substrate 4 Å (Fig. 2 center). With an ITO-coated glass substrate, the RMS surface roughness of a 200 nm-thick film of Al_2O_3 was increased up to 12 Å (Fig. 2 right), which is comparable to the value of the substrate prior to deposition.

So far, we have obtained high-quality Al_2O_3 dielectric insulators with a dielectric constant ($\kappa = 7.5$) almost twice that of SiO_2 . Although, high- κ dielectric insulators are desirable for reducing operating voltage of OFETs, Veres et al. have reported that high- κ dielectrics usually contain polar functional groups that can increase the energetic disorder at the interface, which results in a higher localization of the charge carriers and reduced field-effect mobility in polymer OFETs [12,13]. Recent studies based on organic single-crystal transistors have attributed the dependence of mobility on dielectric polarizability to the coupling/interaction force between the charged carriers in the organic conducting channel and the ionic lattice of the dielectric [14,15]. To minimize the effect of dielectric polar functional groups and other surface charges on the organic conducting channel, the surfaces of all oxides were passivated with an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) just before the deposition of pentacene. It is well established that SAMs applied on the interfaces in OFETs allow for better control of the morphology and properties of the organic semiconducting material. The OTS SAMs were formed by dipping the substrates in a 5 mM toluene solution of OTS for 30 min after the substrates were oxygen-plasma treated for two minutes. The static aqueous contact angle measurement showed that after the treatment, the previously hydrophilic surfaces of both dielectric materials became hydrophobic. A contact angle of 91–92° was obtained from OTS-treated Al_2O_3 on both smooth surface (n^+ -Si) and rough surface (ITO-coated glass), indicating that a uniform self-assembled OTS monolayer with long alkyl chains was formed. This value is slightly lower than that of OTS-treated SiO_2 on n^+ -Si (112°). This can be attributed to a lower concentration of oxygen atoms of Al_2O_3 and a different SAM formation mechanism compared with SiO_2 [16,17].

3. Fabrication and characterization of OFETs with Al_2O_3 gate insulators

OFETs were fabricated using 200 nm-thick Al_2O_3 on n^+ -Si (T1), 200 nm-thick SiO_2 on n^+ -Si

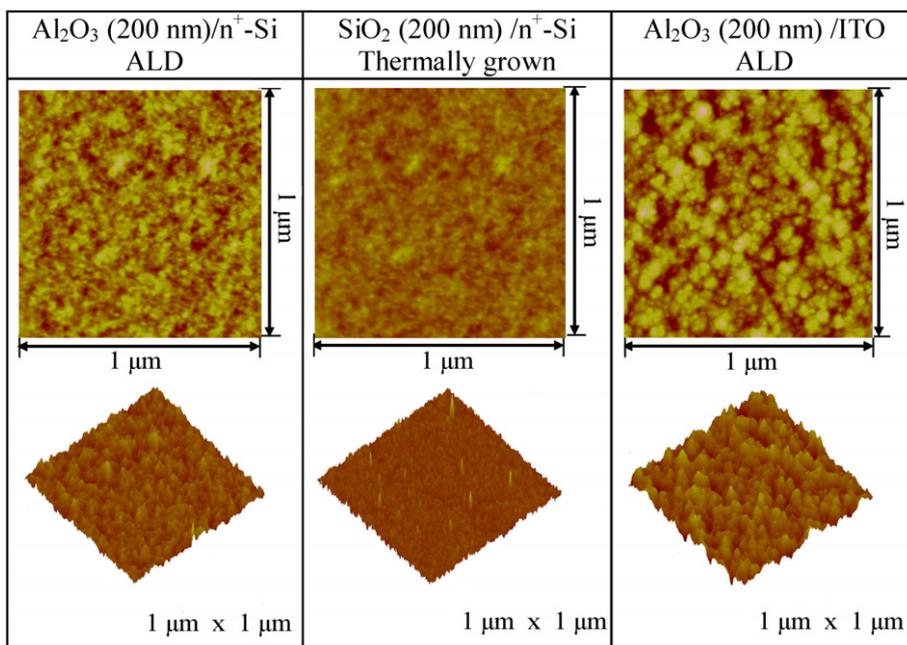


Fig. 2. AFM images ($1\ \mu\text{m} \times 1\ \mu\text{m}$) of a 200 nm-thick Al_2O_3 film grown by ALD on n^+ -Si substrates (left, with a data scale of 5 nm), a 200 nm-thick film of thermally-grown SiO_2 on n^+ -Si substrates (center, with a data scale of 5 nm) and a 200 nm-thick Al_2O_3 film grown by ALD on ITO coated-glass substrates (right, with a data scale of 10 nm).

(T2, the reference sample), and 200 nm-thick Al_2O_3 on ITO-coated glass (T3). All oxide surfaces were treated with OTS SAMs as described above and n^+ -Si and ITO acted as gate electrodes, respectively. All three types of transistors were top-contact devices (as shown in Fig. 3a for T1 and T2, and Fig. 3b for T3). The transistors were fabricated by evaporating a 60 nm-thick film of pentacene on

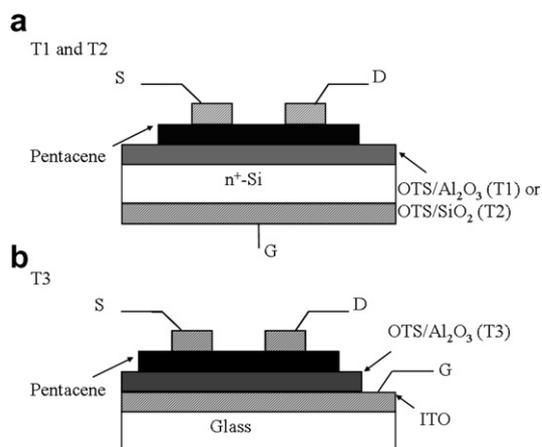


Fig. 3. Diagram of the OFET device geometries for transistors T1 and T2 (a) and T3 (b), where S, D and G stand for source, drain and gate, respectively.

different substrates (T1, T2, and T3) followed by the patterned deposition of a 40 nm-thick Au film capped with a 100 nm-thick Al film to serve as top source/drain electrodes through a shadow mask. Here, a thin Au film was inserted to form a quasi-ohmic contact between pentacene and the source/drain electrodes. Ti/Au (10 nm/100 nm) backside metallization was used as the external gate contact in T1 and T2. Prior to deposition, pentacene (Aldrich) was purified using gradient zone sublimation, and then deposited at a deposition rate of $0.3\ \text{\AA}/\text{s}$, as measured by a crystal monitor. The temperature and pressure during deposition were $25\ ^\circ\text{C}$ and 2×10^{-8} Torr, respectively. The samples were transferred in a vacuum-tight vessel without being exposed to atmospheric conditions into a nitrogen glove box ($\text{O}_2, \text{H}_2\text{O} < 0.1\ \text{ppm}$) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit in a dark environment.

The surface morphology of the pentacene films on different substrates (T1, T2, and T3) was characterized using AFM as shown in Fig. 4. The growth of pentacene films on all three OTS-treated substrates exhibited high structural order and displayed island formation, but no dendrite-like crystal

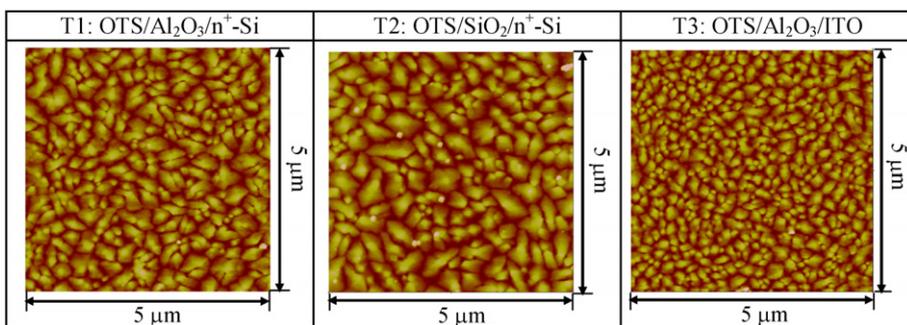


Fig. 4. AFM images ($5 \mu\text{m} \times 5 \mu\text{m}$) of a 60 nm-thick pentacene film on an OTS-treated 200 nm-thick Al_2O_3 film (T1, with n^+ -Si as substrates and gate electrodes), on an OTS-treated 200 nm-thick SiO_2 film (T2, with n^+ -Si as substrates and gate electrodes) and on an OTS-treated 200 nm-thick Al_2O_3 film (T3, with ITO-coated glass as substrates and gate electrodes).

formation was observed. However, the grain size greatly varied from the substrates with different surface energy and surface roughness. Therefore, although the RMS roughness on T1 and T2 are comparable (see Fig. 2), the grain size was slightly reduced on T1 where its aqueous contact angle is lower. A further reduction in grain size can be seen in T3 due to its larger roughness (12 Å) compared to T1 and T2 [18,19]. The larger grain size of pentacene films on T2 may be due to the residual polar groups on SiO_2 , like silanols [20].

Intermolecular layer spacing of pentacene films was determined by X-ray diffraction (XRD). As shown in Fig. 5, the diffraction spectrum of island

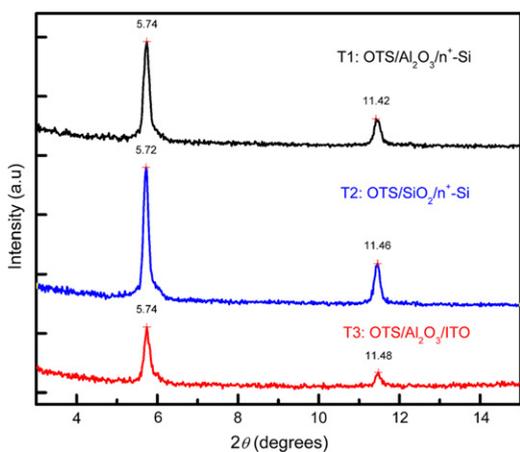


Fig. 5. XRD patterns of a 60 nm-thick pentacene film on an OTS-treated 200 nm-thick Al_2O_3 film (T1, with n^+ -Si as substrates and gate electrodes), on an OTS-treated 200 nm-thick SiO_2 film (T2, with n^+ -Si as substrates and gate electrodes) and on an OTS-treated 200 nm-thick Al_2O_3 film (T3, with ITO-coated glass as substrates and gate electrodes).

films consisted of crystalline peaks with a first diffraction peak at $2\theta = 5.74^\circ$, corresponding to “thin film” spacing of 15.4 Å, and the presence of higher order peaks (up to 4 or 5) was observed on the smooth substrates (T1, T2). The lattice spacing corresponds to a tilt of the molecules of 17.1° to the surface normal, assuming a triclinic single-crystal structure. The presence of a “bulk” phase of pentacene with a spacing of 14.4 Å was not observed for films reported here. Peak intensity and number of higher-order reflections mirrored the grain size of the crystalline structure observed in AFM images: films with larger grains showed higher intensity and more higher-order reflections. With smaller crystalline grain size (Fig. 4), the peak intensity of T1 was slightly lower than that for T2. In comparison, the grain size was reduced and then the peak intensity was decreased in T3 due to its large substrate surface roughness, as discussed by Steudel [18] and Fritz [19].

Pentacene transistors were characterized in the saturation regime defined by standard MOSFET models. To explore the influence of the different dielectrics (Al_2O_3 and SiO_2) on device performance, transistors T1 and T2 with a channel length $L = 65 \pm 5 \mu\text{m}$ and a channel width $W = 590 \pm 90 \mu\text{m}$ were compared. These two types of transistors had similar properties such as substrate surface roughness, pentacene morphology, and structural ordering as discussed earlier. Fig. 6 shows the output characteristics in Fig. 6a (drain-source current I_{DS} vs. drain-source voltage V_{DS} for increasing values of gate-source voltage V_{GS}) and transfer characteristics in Fig. 6b ($-I_{\text{DS}}$ vs. V_{GS} plotted on a logarithmic scale and $\sqrt{|I_{\text{DS}}|}$ vs. V_{GS} , at $V_{\text{DS}} = -30 \text{ V}$) for the two transistors. Field-effect

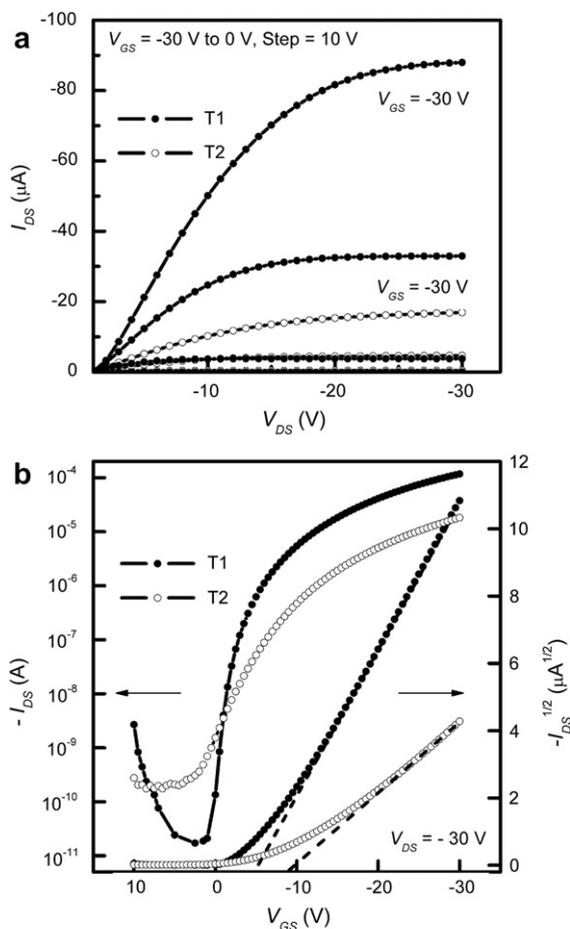


Fig. 6. (a) Output characteristics (I_{DS} vs. V_{DS}) at several values of the gate voltage (V_{GS}) and (b) transfer characteristics ($-I_{DS}$ vs. V_{GS} plotted on a logarithmic scale and $\sqrt{|I_{DS}|}$ vs. V_{GS}) at $V_{DS} = -30$ V for devices ($W = 590 \pm 90 \mu\text{m}$, $L = 65 \pm 5 \mu\text{m}$) with a 60 nm-thick pentacene film on an OTS-treated 200 nm-thick Al_2O_3 film (T1) and an OTS-treated 200 nm-thick SiO_2 film (T2), with n^+ -Si as substrates and gate electrodes.

mobilities and threshold voltages were calculated in the saturation regime by fitting the $\sqrt{|I_{DS}|}$ vs. V_{GS} data to the square law:

$$I_{DS} = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \quad (1)$$

where μ is the field-effect mobility, C_{OX} is the capacitance density of the gate dielectric insulator, V_T is the threshold voltage, and W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes.

A field-effect mobility of $1.5 \pm 0.2 \text{ cm}^2/\text{V s}$ was extracted for the T1 transistors while the T2 transistors had a lower carrier mobility of $0.6 \pm 0.1 \text{ cm}^2/\text{V s}$. With Al_2O_3 ($\kappa = 7.5$) as gate insulators, the

capacitance density of the gate insulator in T1 transistors was as high as $32.7 \text{ nF}/\text{cm}^2$ as compared to $17.3 \text{ nF}/\text{cm}^2$ in T2 transistors. Consequently, the saturation current ($-88 \mu\text{A}$) in T1 transistors was almost five times larger than that ($-17 \mu\text{A}$) obtained from T2 transistors as shown in Fig. 6a. The higher mobility and current obtained from T1 transistors can be correlated with the morphology of pentacene film and the dielectric/surface properties of OTS-treated Al_2O_3 : first, compared with pentacene films on T2 (OTS-treated SiO_2), a reduced grain size and a well-ordered island formation of pentacene films on OTS-treated Al_2O_3 (T1) indicate a higher interconnection and tighter packing (with improved contact) between grains, which could lead to more efficient charge transport and enhance the drain current in the channel [21]. Secondly, with OTS SAMs on the surface, the surface disorder induced by the polar groups from high- κ dielectric surface (Al_2O_3 in our case) can be minimized. This is confirmed by the zero turn-on voltage V_{TO} shown on the transfer curve in Fig. 6b, indicating that no net fixed charges exist at the semiconductor/insulator interface. By using gate insulators with higher dielectric constant, a higher concentration of the charge carriers is accumulated in the channel for the same gate voltage and the Fermi level moves towards the band edge. The trapping states located in the ‘gap’ are filled and consequently a higher density of injected carriers is free to move with the microscopic mobility associated with carriers in the delocalized states. Thus, the use of high- κ dielectrics not only lowers the operating voltage, but also improves the mobility. This increase in mobility can be superlinear, as observed in this study, since it is due to the cumulative process of carriers becoming available at higher energies as the lower energy traps are filled. Using dielectric films with comparable thickness but having different dielectric constants, Dimitrakopoulos et al. have demonstrated that the mechanism responsible for enhancing TFT carrier mobility is related to the carrier density in the channel region rather than the gate electric field [22].

Along with a zero turn-on voltage V_{TO} , a low threshold voltage of -7 ± 2 V and a subthreshold slope of 0.6 V/decade were extracted for T1. A high on/off current ratio of 6×10^6 was also obtained for T1, measured between the ‘on’ current value at $V_{GS} = -30$ V and the ‘off’ current at $V_{GS} = 0$ V, both with $V_{DS} = -30$ V. On the other hand, T2 showed a positive turn-on voltage V_{TO} of 5 V with a threshold voltage of -9 ± 2 V. Thus the transis-

tors were operated in the depletion mode instead of the enhancement mode as in T1, and consequently they could only be switched off by applying a positive gate bias. In addition, a higher sub-threshold slope of 3 V/decade and a lower on/off ratio of 10^5 were obtained for T2. The “off” current in T2 was 10 times higher than that in T1. These significant improvements in subthreshold slope, turn-on voltage (threshold voltage) and “off” current seen in T1 transistors can be attributed to a lower charge trap density at the pentacene/dielectric interface. We can estimate the maximum interfacial trap density $N_{\text{trap}}^{\text{max}}$ from Eq. (2): [23,24]

$$N_{\text{trap}}^{\text{max}} = \frac{C_{\text{OX}}}{q} \left[\frac{qS \log e}{k_{\text{B}}T} - 1 \right] \quad (2)$$

where k_{B} is Boltzmann’s constant, T is temperature, q is the electronic charge, e is the base of the natural logarithm, C_{OX} is the capacitance density of the gate insulator and S is the subthreshold slope in V/decade. Calculated from Eq. (2), the trap density at the OTS-treated Al_2O_3 (T1) surface was as low as $1.8 \times 10^{12} \text{ cm}^{-2}$. A much higher value of trap density ($5.2 \times 10^{12} \text{ cm}^{-2}$) was obtained from OTS-treated SiO_2 (T2) surface. This higher value can explain the positive turn-on voltage, larger subthreshold slope, and higher “off” current observed in T2. However, this calculated trap density value for OTS-treated SiO_2 is comparable to previously reported values for bare SiO_2 [23]. The interfacial traps are usually due to surface imperfections such as oxygen (OH groups), water molecules or mobile ions. It has been shown that silanol groups on SiO_2 cannot be completely passivated by self-assembled alkyl layers [25]. The residual silanol groups can trap electrons with protons and release H_2 , therefore forming negative charges and inducing a positive shift in V_{TO} [20]. The electrical parameters we discussed here for transistors T1 and T2 along with those of the transistors T3 to be discussed next are summarized in Table 1.

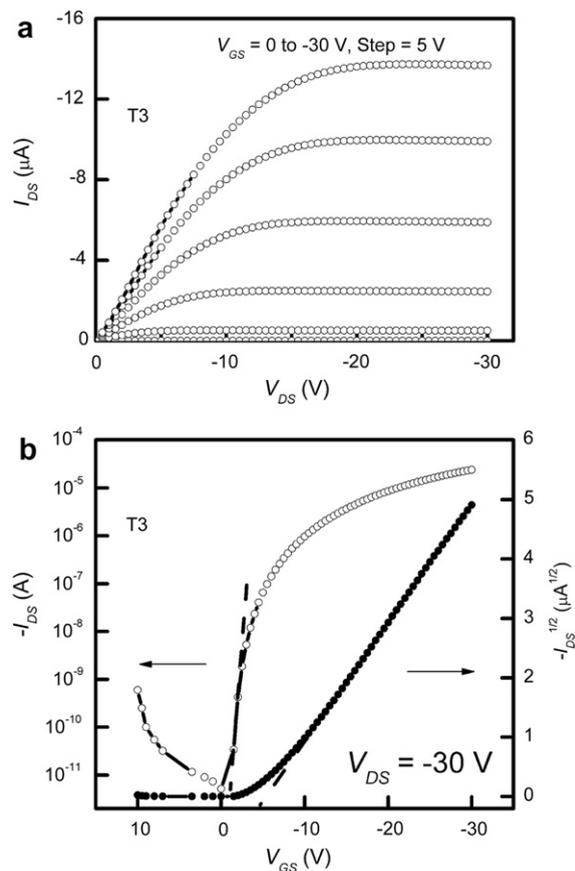


Fig. 7. (a) Output characteristics (I_{DS} vs. V_{DS}) at several values of the gate voltage (V_{GS}) and (b) transfer characteristics ($-I_{\text{DS}}$ vs. V_{GS} plotted on a logarithmic scale and $\sqrt{|I_{\text{DS}}|}$ vs. V_{GS}) at $V_{\text{DS}} = -30 \text{ V}$ for devices ($W = 550 \pm 50 \mu\text{m}$, $L = 185 \pm 5 \mu\text{m}$) with a 60 nm-thick pentacene film on an OTS-treated 200 nm-thick Al_2O_3 film with ITO as substrates and gate electrodes (T3).

The output characteristics and transfer characteristics of T3 transistors were shown in Figs. 7a and 7b, respectively. Even though the substrate ITO-coated glass had a relatively large surface roughness (see Fig. 2), a high field-effect mobility of $0.9 \pm 0.1 \text{ cm}^2/\text{V s}$ was obtained in the saturation region for T3 (Fig. 7b) with a channel length

Table 1

Summary of the electrical parameters for pentacene transistors T1, T2, and T3

Transistors	t (nm)	C_{OX} (nF/cm ²)	μ (cm ² /V s)	V_{T} (V_{TO}) (V)	S (V/decade)	$N_{\text{trap}}^{\text{max}}$ ($\times 10^{12} \text{ cm}^{-2}$)	$I_{\text{on/off}}$
T1: OTS/ $\text{Al}_2\text{O}_3/n^+$ -Si	200	32.7	1.5 ± 0.2	-7 ± 2 (0)	0.6	1.8	6×10^6
T2: OTS/ SiO_2/n^+ -Si	200	17.3	0.6 ± 0.1	-9 ± 2 (5)	3	5.2	10^5
T3: OTS/ Al_2O_3 /ITO	200	32.7	0.9 ± 0.1	-6 ± 1 (0)	0.5	1.4	10^6

t : thickness of gate dielectric insulator, C_{OX} : capacitance density, μ : carrier mobility, V_{T} : threshold voltage, V_{TO} : turn-on voltage, S : sub-threshold slope, $N_{\text{trap}}^{\text{max}}$: maximum interfacial trap density, $I_{\text{on/off}}$: on/off current ratio.

$L = 185 \pm 5 \mu\text{m}$ and a channel width $W = 550 \pm 50 \mu\text{m}$. This value of mobility ranks to date as the highest known mobility reported for pentacene-based OFETs on ITO-coated glass [26]. This indicates that the contribution of higher carrier density to the field-effect mobility is dominant compared to the adverse effect of the substrate roughness on the morphology and transport. In addition to the high-mobility values, T3 transistors exhibited superior electrical characteristics similar to those of T1: a turn-on voltage V_{TO} of zero volts, a threshold voltage of $-6 \pm 1 \text{ V}$, and a subthreshold slope of 0.5 V/decade, as extracted from the transfer characteristic curve (Fig. 7b). The maximum trap density was estimated to be $1.4 \times 10^{12} \text{ cm}^{-2}$, which is again close to the value estimated for T1. The consistency of trap density across the same type of oxide surface further confirms that Al_2O_3 has fewer trapping sites. A high on/off current ratio larger than 10^6 was also obtained from T3. Since pentacene growth, and thus OFETs made of it, can be affected by the roughness of dielectric layers underneath as demonstrated by Fritz et al. [19], the high performance of T3 transistors demonstrates the effectiveness of employing an Al_2O_3 layer grown by ALD technique as a dielectric for inherently rough substrates.

4. Conclusions

In summary, we have utilized atomic layer deposition (ALD) to grow Al_2O_3 gate dielectric insulators and obtained high-performance pentacene OFETs. OFETs fabricated on n^+ -Si wafers and ITO-coated glass were operated in enhancement mode with a zero turn-on voltage, and exhibited large carrier mobility and a low threshold voltage, as well as a low subthreshold slope and a large on/off current ratio. Atomic force microscopy (AFM) images of pentacene films on Al_2O_3 revealed well-ordered island formation, and X-ray diffraction patterns showed characteristics of a “thin film” phase. Low trap density and high capacitance density of Al_2O_3 gate insulators also contributed to the high performance of pentacene field-effect transistors. The results of this work not only demonstrate that gate dielectrics grown by ALD present a viable alternative to dielectrics from traditional deposition techniques, but also show that the ALD dielectrics can result in improved electrical performance of transistors even on substrates with high roughness. The latter will become an increas-

ingly critical issue in future for most flexible substrates of interest.

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